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IMPACT OF INPUT EMI FILTER DESIGN ON THE DYNAMIC PERFORMANCE OF AVERAGE-CURRENT-MODE CONTROLLED BOOST CONVERTER

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ABSTRACT

Jia Wang: Impact of Input EMI Filter Design on the Dynamic Performance of Average-Current-Mode Controlled Boost Converter
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An input EMI filter is usually employed for dealing with electromagnetic interference (EMI) caused by the switching actions of switched-mode converters. However, the existence of the input filter often interacts with the connected converter, thus leads to performance degradation and even stability issues. This thesis presents a thorough case study that focuses on the impact of the design of the input EMI filter parameters—one of the main factors that affect the adverse filter-converter interaction—on the dynamic response of the filter-converter interconnected system. A switched-mode boost converter under average-current-mode (ACM) control operates in continuous conduction mode (CCM) is utilized as an example. With the purpose of analyzing the stability of the aforementioned converter cascaded with different sized input filters, the impedance-based stability assessment method is used by utilizing the Nyquist stability criterion (NSC) on the impedance ratio of this interconnected system. To identify this minor loop gain, small-signal models that represent the dynamic behaviors are constructed for the ACM controlled DC-DC boost converter as well as the input EMI filter. Furthermore, to validate theoretical results, input filters are designed in different sizes with the MATLAB environment. To this end, damping circuits are added to solve the problems caused by filter-converter interactions. Simulation results are provided to demonstrate the correctness of the obtained small-signal models, as well as the correspondence between the predictions of impedance-based stability assessment and the transient performance of the cascaded system.

Keywords: Filter-converter interaction, Average-current-mode control, Boost converter, Dynamic modeling, impedance-based stability criterion

PREFACE

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Jia Wang

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LIST OF SYMBOLS AND ABBREVIATIONS

AC	Alternating Current
ACM	Average Current Mode
CCM	Continuous Conduction Mode
CMC	Current Model Control
DC	Direct Current
DCM	Discontinuous Conduction Mode
DDR	Direct Duty Ratio
EMI	Electromagnetic Interference
ESR	Equivalent Series Resistance
GM	Gain Margin
LHP	Left Half Plane
LTI	Linear Time Invariant
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
NSC	Nyquist Stability Criterion
PCM	Peak Current Mode
PI	Proportional Integral
PID	Proportional Integral Derivative
PM	Phase Margin
PWM	Pulse-Width Modulation
RHP	Right Half Plane
SSA	State Space Averaging
TAU	Tampere University
TUNI	Tampere Universities
URL	Uniform Resource Locator
VF	Voltage-fed
VMC	Voltage Mode Control

$\mathbf{C_f}$	Capacitor of the input filter
$\mathbf{C}$	Capacitor
$\frac{\mathbf{d}}{\mathbf{dt}}$	Derivative of the variable
$\mathbf{d}$	Duty Ratio
$\hat{\mathbf{d}}$	Perturbed duty Ratio
$\mathbf{D}$	Steady-state duty Ratio
$\mathbf{f_{co-minor}}$	Crossover frequency of the minor loop gain
$\mathbf{f_{co}}$	Crossover frequency

$\mathbf{F_m}$	Duty ratio gain
$\mathbf{f_{res}}$	Resonant frequency
$\mathbf{f_s}$	Switching frequency
$\mathbf{G_{ci-o}}$	Control-to-input transfer function
$\mathbf{G_{co-o}}$	Control-to-output transfer function
$\mathbf{G_{con}(s)}$	Controller transfer function
$\mathbf{G_{io-o}}$	Forward transfer function
$\mathbf{G_{ij-\infty}}$	Ideal transfer functions
$\mathbf{G_{PWM}}$	Pulse-width modulator gain
$\mathbf{G_{c-i}}$	Transfer function of the inductor current controller
$\mathbf{G_{c-v}}$	Transfer function of the output voltage controller
$\mathbf{G(s)}$	Transfer function
$\mathbf{H_i}$	Inductor current sensing gain
$\mathbf{H_v}$	Output voltage sensing gain
$\mathbf{H(s)}$	Sensing transfer function
$\mathbf{i_C}$	Capacitor current
$\mathbf{i_{L-ripple}}$	Inductor current ripple
$\mathbf{i_L}$	Inductor current
$\mathbf{i_{in}}$	Input current
$\mathbf{I_{L-pp}}$	Maximum allowed peak-to-peak inductor current ripple
$\mathbf{I_o}$	Ideal current sink
$\langle \mathbf{i_L} \rangle$	Time-averaged inductor current
$\mathbf{K}$	Control Gain
$\mathbf{K_{minor}}$	Minor loop gain
$\mathbf{L_{v-damped}}$	Damped-filter-affected control loop gain
$\mathbf{L_{DDR}}$	Direct-duty-ratio control loop gain
$\mathbf{L_{v-f}}$	Filter-affected voltage control loop gain
$\mathbf{L_f}$	Inductor of the input filter
$\mathbf{L}$	Inductor
$\mathbf{L_i}$	Input current control loop gain
$\mathbf{L_v}$	Output voltage control loop gain
$\mathbf{M_{PWM}}$	Constant-slope of the PWM signal
$\mathbf{m_2}$	Negative down-slope of the inductor current
$\mathbf{m_1}$	Positive up-slope of the inductor current
$\mathbf{r_{Cf}}$	Equivalent series resistance of filter capacitor
$\mathbf{r_{Lf}}$	Equivalent series resistance of filter inductor
$\mathbf{r_C}$	Equivalent series resistance of the capacitor
$\mathbf{r_L}$	Equivalent series resistance of the inductor

$\mathbf{r_d}$	Parasitic resistance of the diode
$\mathbf{r_{ds}}$	Parasitic resistance of the transistor
$\mathbf{R}$	Resistor
$\mathbf{R_s}$	Sensing resistor for the inductor current
$\mathbf{t_{off}}$	Off-time of a switching cycle
$\mathbf{t_{on}}$	On-time of a switching cycle
$\mathbf{T_{oi-o}}$	Reverse transfer function
$\mathbf{T_s}$	Switching cycle time
$\mathbf{U}(\mathbf{s})$	Laplace transformation of input variables
$\mathbf{v_C}$	Capacitor voltage
$\mathbf{V_D}$	Forward voltage drop on diode
$\mathbf{v_L}$	Inductor voltage
$\mathbf{V_{in}}$	Input voltage
$\mathbf{V_M}$	Magnitude of the PWM ramp
$\mathbf{V_{C-ripple}}$	Maximum allowed output voltage ripple
$\mathbf{v_{ca}}$	Output signal of the current compensator
$\mathbf{v_{co}}$	Output signal of the voltage compensator
$\mathbf{v_o}$	Output voltage
$\mathbf{V_{o-ref}}$	Reference of the output voltage
$\mathbf{V_C}$	Steady-state capacitor voltage
$\mathbf{V_L}$	Steady-state inductor voltage
$\mathbf{V_{dip}}$	Voltage dip
$\mathbf{X}(\mathbf{s})$	Laplace transformation of state variables
$\mathbf{Y_{in-o}}$	Converter input admittance
$\mathbf{Y}(\mathbf{s})$	Laplace transformation of output variables
$\mathbf{Y_L}$	Load admittance
$\mathbf{Y_{in-sco}}$	Short-circuit input admittance
$\mathbf{Z_{in-o}}$	Converter input impedance
$\mathbf{Z^o_{o-oci}}$	Open-circuit output impedance
$\mathbf{Z_{o-o}}$	Output impedance of the converter
$\mathbf{Z_{of}}$	Output impedance of the input-filter
$\mathbf{Z_S}$	Source impedance
$\mathbf{Z_{of-damp}}$	Total impedance of the damped-input-filter
$\omega_{\mathbf{pole}}$	Pole in frequency-domain
$\omega_{\mathbf{res}}$	Resonant frequency in frequency-domain
$\omega_{\mathbf{n}}$	Undamped natural frequency
$\omega_{\mathbf{zero}}$	Zero in frequency-domain
ζ	Damping factor

1 INTRODUCTION

As one of the main technicals for power conversion with high frequency, power electronics achieved desired control goals by combining solid-state semiconductor power devices and circuits with a control system [35]. However, power electronics is facing challenges with the rapid development of technology, one of them is how to minimize the harmful interactions between the electronic equipment [35], for instance, the interactions between input electromagnetic interference (EMI) filter and switched-mode converters. While considerable research related to dynamic behaviors of converters [8, 16, 17, 22, 30] and filter-converter interactions [13, 15, 27, 33] have been done in the past, the comprehensive case study that focuses on the impact of filter design on the converter performance as well as stability analysis of filter-converter interconnected system is inadequate.

The reason for using the input EMI filter is that the harmful EMI generated by the switching actions of the switched-mode converters needs to be removed. Typically, the switched-mode converters are controlled by active elements that support high-frequency switching action. However, the active switches can be an origin of EMI due to the switching behavior of these active switches. This EMI will lead to harmonic resonance, poor power quality, and even instability. Additionally, the switching frequency is getting higher and higher due to technological improvements of the active switches. Although this change reduces the size of passive components, it increases the generated EMI level as well. Thus, an input EMI filter is indispensable to be connected to the converter. [5]

Although the input filter is capable to reduce the generated EMI level, an improperly tuned input filter may affect the converter response, causing performance degradation and even instability [13]. This thesis focuses on the stability analysis of the filter-converter interconnected system founded on dynamic modeling by presenting a practical case study of the Average-current-mode (ACM) controlled DC-DC boost converter. To achieve this goal, the impedance ratio, i.e., the minor loop gain that consists of the output impedance of the input EMI filter as well as the converter input impedance at closed loop, is required to assess the stability of this cascade-connected system by utilizing the Nyquist Stability Criterion (NSC) on it [29, p.12]. This evaluation approach is called impedance-based stability analysis method. Correspondingly, the system stability predicted by the impedance-based stability approach is verified with simulation results in MATLAB. In addition, the performance degradation and stability issues caused by the input filter can be avoided by connecting a damping circuit with it.

In order to compute the minor loop gain, small-signal models that represent the dynamic behaviors (i.e., transfer functions that depict the internal dynamical properties) of the closed loop converter need to be constructed with the help of two-port model and control block diagram [8]. This constructing process is known as dynamic modeling. From this modeling perspective, a standard procedure for modeling the DC-DC converters (i.e., State-Space Averaging (SSA) method developed in 1976) for studying the dynamics of power converters [19]. However, this SSA method only works in the Direct Duty Ratio (DDR), also known as Voltage Mode Control (VMC), controlled converters that operate in Continuous Conduction Mode (CCM) [29, p. 7]. To model the converters under other control methods, for example, the Current Mode Control (CMC) used in this thesis, the small-signal dynamic model can be computed on the basis of the small-signal model under DDR control, in which the generated duty ratio is affected by the internal feedback loop [29, p. 57]. It is noticeable that careful control design (i.e., designing the compensator transfer functions with loop shaping techniques) is required to assure the stable operation of the converter.

This structure of this thesis is presented in the following manner: the theoretical background of the thesis, including the State Space Averaging (SSA) method, system dynamic response and impedance-based stability analysis method is addressed in Chapter 2. Chapter 3 provides an introduction to Current Mode (CM) and Direct-Duty-Ratio (DDR) control techniques for switched-

mode converters, and the dynamic models of the boost converter under each control method. Accordingly, Chapter 4 implemented the DDR and ACM control design in the Simulink environment. Chapter 5 introduces the dynamic models of the filter-affected converter as well as minor loop gain computation. Simulation results that display how the filter design affects the control performance are addressed in Chapter 6. Chapter 7 gives not only the drawn conclusion but also suggestions for future studies.

2 THEORETICAL BACKGROUND

This chapter introduces the essential background information behind generalized dynamic analysis using State-Space Averaging (SSA) method as well as presents the open loop transfer function matrix of the boost converter. Additionally, this chapter provides a comprehensive introduction to the system frequency response, transient response and system characteristics that need to be noticed in the system dynamics.

2.1 Working Principle of the DC-DC Boost Converter

Power electronic converters can be classified into four types, Alternating current-Direct current (AC-DC), AC-AC, DC-DC, and DC-AC converters. The DC-DC switched-mode converters, as the most fundamental category, are frequently used in many applications that require well-regulated output DC voltage. A boost converter enables transforming the energy that stored in the passive elements to the output side at a higher level than the input side [6]. Figure 2.1 illustrates the power stage of the Voltage-fed (VF) DC-DC switched-mode boost converter studied in this thesis.

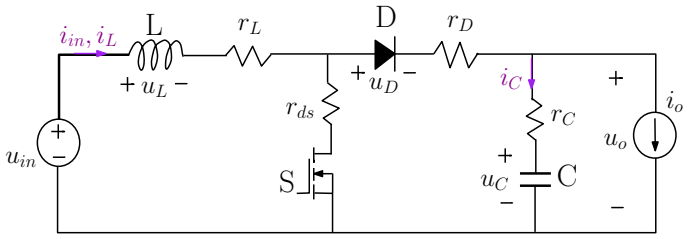


Figure 2.1. *Power stage of a voltage-fed PWM DC-DC switched-mode boost converter*

Three operation modes are available for the converters, continuous (CCM), boundary (BCM), and discontinuous (DCM) conduction mode. As CCM is commonly used and easier to analyze than DCM, the PWM boost converter in this case works in CCM, where the inductor current has two slopes in opposite direction within a switching cycle and it does not drop to zero [26, p. 68].

As Figure 2.1 depicts, this boost converter comprised of an ideal Direct current (DC) voltage source (V_{in}), necessary passive components including a capacitor (C) and an inductor (L), an ideal current sink (I_o) as the load and switching components (i.e., a metal-oxide-semiconductor field-effect transistor (MOSFET) and a diode which prevents current flowing back into the source when MOSFET is conducting). The switching losses of the switching components are represented by the parasitic resistances (r_{ds} and r_D). In addition, the switching harmonics are neglected because the switching ripple in the voltage is small in a well-constructed converter [5].

2.2 State-Space Averaged Model of Boost Converter

SSA method for establishing the analytical transfer functions is introduced in this section. By linearizing the averaged model at steady-state operating points, the small-signal model can be constructed. The derived linear time-invariant (LTI) models are precise in the frequencies up to half of the converter switching frequency [32]. This method is applicable when the converter operates in CCM.

2.2.1 Basic Procedure of Small-Signal Modeling

Generally, the dynamic analysis starts with recognizing the proper input, output, control, and state variables. The variables at the input side are normally represented by the main electrical variables of the sources that are connected to the terminals, they can be controllable inputs, natural inputs or disturbances [29, p. 57]. The output variables are all the variables we intend to solve, which are the most often the duals of the input variables. The capacitor voltage and inductor current are usually selected as the state variables due to their storage element nature [29, p. 57]. The SSA method means that these instantaneous variables are averaged within a single switching cycle, producing the average model of the corresponding converter.

Additionally, the small-ripple approximation is used to define average models of the corresponding converter, which simplified the analysis by applying the average DC values of the state variables for all switching states, because the ripple existing in the output voltage of converter is only a few percent of the nominal value, which means it is negligible [5]. As a result, the derivatives of the output variables and the state variables are demonstrated as functions of control, input, and state variables. Then the linearizing technique is applied at a certain operating point on the average model to obtain the small-signal models which are valid merely in the region of low-frequency (i.e., up to half the converter switching frequency) because of the nature of averaging [29, p. 57].

Dynamic modeling with regards to power electronic converters relies on the use of Laplace transformation, which is very useful for obtaining transfer functions by transfer variables from time-domain to frequency-domain. Although Average Current Mode (ACM) Control is applied instead of Direct Duty Ratio (DDR) control, the closed loop dynamic model under ACM control can be established based on the basic dynamic models under DDR control by substituting a proper duty ratio constraint for the perturbed duty ratio [29, p. 57-59].

2.2.2 Averaged Steady-State Model of Boost Converter

Averaging the DC-DC converter operation within a single switching cycle is a commonly used approach to remove the nonlinearity nature of the power electronic converter caused by the periodically switching actions [29, p. 129]. The dynamic behaviors in a VF converter depends mostly on the behavior of time-averaged inductor current $\langle i_L \rangle$. Figure 2.2 displays a portion of i_L in a single switching cycle, which has positive up-slope (m_1) as well as negative down-slope (m_2). The up-slope is the local average within the on-time (t_{on}) while the down-slope is the local average within the off-time (t_{off}). [29, p. 129]

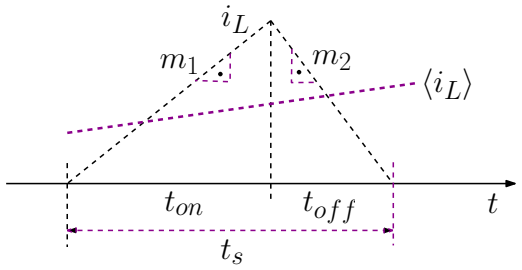


Figure 2.2. *Inductor current waveforms in a single switching cycle*

According to Figure 2.2, the time-averaged inductor current $\langle i_L \rangle$ within the subcycles can be presented as:

$$\begin{aligned} \langle i_L \rangle_{on} &= \frac{t_{on}}{t_{on} + t_{off}} \langle i_L \rangle \\ \langle i_L \rangle_{off} &= \frac{t_{off}}{t_{on} + t_{off}} \langle i_L \rangle \end{aligned} \tag{2.1}$$

Furthermore, the derivative of time-averaged inductor current $\langle i_L \rangle$ is computed as Equation

(2.2) approximately [29, p. 130].

$$\frac{d\langle i_L\rangle_{on}}{dt} = \frac{t_{on}}{t_s}m_1 - \frac{t_{off}}{t_s}m_2 \tag{2.2}$$

For developing the state space, sub-circuit structures of the boost converter need to be identified during the on and off times to construct the state, input and output variables. The control variable, duty ratio $d = \frac{t_{on}}{t_s}$, is implemented by the transistor that switches at the switching frequency f_s.

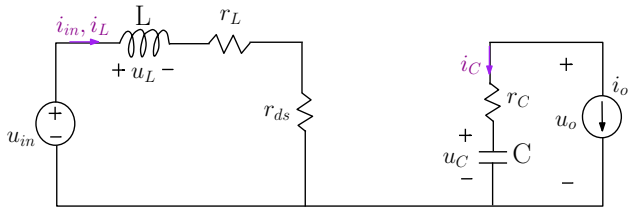


Figure 2.3. *Power stage of the boost converter during on-time*

As given in Figure 2.3, when the MOSFET is switched on, the DC voltage source charges the inductor while the capacitor is discharging. In such a situation, the transistor is assumed to have mainly resistive losses when it is fully conducting, i.e, it is modeled as a resistance r_{ds}. The on-time equations are as follows:

$$\begin{aligned} V_L &= V_{in} - r_L i_L - r_{ds} i_L \\ V_C &= V_o - r_C i_C \\ i_C &= -i_o \\ i_{in} &= i_L \end{aligned} \tag{2.3}$$

Where the time-varying average inductor current is represented by i_L, v_C denotes the time-varying average capacitor voltage.

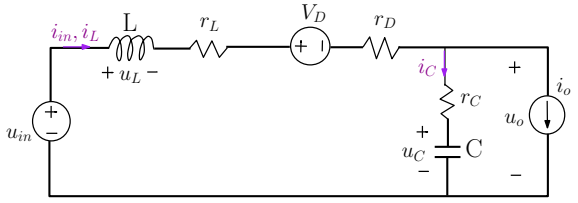


Figure 2.4. *Power stage of the DC-DC boost converter during off-time*

In contrast, the diode conducts while the MOSFET is switched off as demonstrated in Figure 2.4, the inductor starts discharging and feed both the capacitor and the load. Diode is modeled as a voltage-drop V_D and a resistance r_D. The off-time equations are as follows:

$$\begin{aligned} V_L &= V_{in} - r_L i_L - r_D i_L - V_D - r_C i_C - V_c \\ V_C &= V_o - r_C i_C \\ i_C &= i_L - i_o \\ i_{in} &= i_L \end{aligned} \tag{2.4}$$

According to the sub-circuit equations above, the averaged state-space model can be computed by applying the principle of averaging over a single switching cycle as presented in Equation (2.5). We can obtain the information on the average voltage across the inductor by summing the product the duty ratio d and the on-time inductor voltage v_{L-on} together with the product of the inverse of duty ratio ($d^{'}$) and the off-time inductor voltage v_{L-off}. The average current that flowing

through the capacitor is acquired in the same way.

$$\begin{aligned}\frac{d\langle i_L\rangle}{dt} &= \frac{1}{L}(dv_{L-on} + d^{'}v_{L-off}) \\ \frac{d\langle v_C\rangle}{dt} &= \frac{1}{C}(di_{C-on} + d^{'}i_{C-off})\end{aligned} \tag{2.5}$$

Assume that the diode voltage drop is considered as constant. The averaged state-space model is shown in Equation 2.6 and the "⟨⟩" around the variables denotes the average value [29, p. 146]:

$$\begin{aligned}\frac{d\langle i_L\rangle}{dt} &= \frac{1}{L}[\langle v_{in}\rangle + d^{'}r_c\langle i_o\rangle - (r_L + dr_{ds} + d^{'}r_D + d^{'}r_C)\langle i_L\rangle - d^{'}v_C - d^{'}V_D] \\ \frac{d\langle v_C\rangle}{dt} &= \frac{1}{C}[d^{'}i_L - i_o] \\ \langle i_{in}\rangle &= \langle i_L\rangle \\ \langle v_o\rangle &= \langle v_C\rangle - r_C\langle i_o\rangle + d^{'}r_C\langle i_L\rangle\end{aligned} \tag{2.6}$$

From the comparison between the derivative of time-averaged inductor current $\langle i_L\rangle$ expression in Equation (2.2) and in averaged state space, the up-slope and down-slope can be computed as below. Noticing that $d = \frac{t_{on}}{t_s}$ and its inverse $d^{'} = \frac{t_{off}}{t_s}$.

$$\begin{aligned}m_1 &= \frac{\langle v_{in}\rangle - (r_L + r_{ds})\langle i_L\rangle}{L} \\ m_2 &= \frac{(r_L + r_D + r_C)\langle i_L\rangle + \langle v_C\rangle - r_C\langle i_o\rangle + V_D - \langle v_{in}\rangle}{L}\end{aligned} \tag{2.7}$$

2.2.3 Linearized Steady-State Model

For the purpose of finding the initial values to start the transient analysis, steady-state operating points are determined by assuming all derivative terms are zero at first, then substituting the corresponding DC values into averaged variables, yielding solved Inductor current, capacitor voltage, output current, and duty ratio as illustrated below.The averaged model can predict the low-frequency behavior of the output variables of the converter (i.e., input current as well as output voltage) [5]. Applying linearization techniques to the obtained averaged model at the steady-state operating point further yields the expected dynamic representation of the boost converter [29, p. 129].

$$\begin{aligned}I_L &= \frac{I_o}{D^{'}} \\ I_{in} &= I_L \\ V_o &= V_C \\ V_C &= \frac{V_{in} - D^{'}V_D}{D^{'}} - \frac{r_L + Dr_{ds} + D^{'}r_D + DD^{'}r_C}{D^{'2}}I_o \\ (V_o + V_D - r_C I_o)D^{'2} &- [V_{in} - (r_D - r_{ds} + r_C)I_o]D^{'} + (r_L + r_{ds})I_o = 0\end{aligned} \tag{2.8}$$

To achieve the dynamic analysis of the converters in frequency-domain, Laplace transformation is required. However, the averaged state space is a nonlinear model while Laplace transformation can be applied only for linear systems. Therefore, the first-order Taylor's approximation is used to linearize the averaged model because the first-order derivative gives adequate accuracy on how the AC signals behave around the operating point [5]. The input variables of the converter are input voltage (v_{in}) and output current (i_o) while the variables at the output side are the input current (i_{in}) and output voltage (v_o). The capacitor voltage (v_C) as well as inductor current (i_L) are defined as state variables and duty ratio (d) is employed as the control variable. The linearized state-space model is expressed as Equation 2.9 and the "^" over the variables indicates their

small-signal nature:

$$\begin{aligned}
\frac{d\hat{i}_L}{dt} &= \frac{1}{L}[\hat{v}_{in} - r_1\hat{i}_L - D^{'}\hat{v}_C + D^{'}r_C\hat{i}_o + V_1\hat{d}] \\
\frac{d\hat{v}_C}{dt} &= \frac{1}{C}[D^{'}\hat{i}_L - \hat{i}_o - I_L\hat{d}] \\
\hat{i}_{in} &= \hat{i}_L \\
\hat{v}_o &= \hat{v}_C + r_C(D^{'}\hat{i}_L - \hat{i}_o - I_L\hat{d})
\end{aligned} \tag{2.9}$$

where

$$\begin{aligned}
r_1 &= r_L + Dr_{ds} + D^{'}r_D + D^{'}r_C \\
V_1 &= V_o + V_D + (r_D - r_{ds} + Dr_C)\frac{I_o}{D^{'}}
\end{aligned} \tag{2.10}$$

This matrix formed linearized state space in time-domain is given as:

$$\begin{aligned}
\begin{bmatrix} \frac{d\hat{i}_L}{dt} \\ \\ \frac{d\hat{v}_C}{dt} \end{bmatrix} &= \underbrace{\begin{bmatrix} -\frac{r_1}{L} & -\frac{D^{'}}{L} \\ \\ \frac{D^{'}}{C} & 0 \end{bmatrix}}_{\mathbf{A}} \begin{bmatrix} \hat{i}_L \\ \\ \hat{v}_C \end{bmatrix} + \underbrace{\begin{bmatrix} \frac{1}{L} & \frac{D^{'}r_C}{L} & \frac{V_1}{L} \\ \\ 0 & -\frac{1}{C} & -\frac{I_L}{C} \end{bmatrix}}_{\mathbf{B}} \begin{bmatrix} \hat{v}_{in} \\ \\ \hat{i}_o \\ \\ \hat{d} \end{bmatrix} \\
\begin{bmatrix} \hat{i}_{in} \\ \\ \hat{v}_o \end{bmatrix} &= \underbrace{\begin{bmatrix} 1 & 0 \\ r_C D^{'} & 1 \end{bmatrix}}_{\mathbf{C}} \begin{bmatrix} \hat{i}_L \\ \\ \hat{v}_C \end{bmatrix} + \underbrace{\begin{bmatrix} 0 & 0 & 0 \\ 0 & -r_C & -r_C I_L \end{bmatrix}}_{\mathbf{D}} \begin{bmatrix} \hat{v}_{in} \\ \\ \hat{i}_o \\ \\ \hat{d} \end{bmatrix}
\end{aligned} \tag{2.11}$$

2.2.4 Open-Loop Transfer Function Matrix

For solving the transfer functions of the boost converter, Laplace transformation is further utilized to the linearized state space (Equation 2.9) to transfer it from time-domain to frequency-domain, which is easier to investigate the performance of the converter. Because Laplace transform enables to transform differential equations into algebraic form which is easier to manipulate [7, p. 93]. The generalized linearized state-space expression in frequency-domain is constructed as:

$$\begin{aligned}
s\mathbf{X}(s) &= \mathbf{A}\mathbf{X}(s) + \mathbf{B}\mathbf{U}(s) \\
\mathbf{Y}(s) &= \mathbf{C}\mathbf{X}(s) + \mathbf{D}\mathbf{U}(s)
\end{aligned} \tag{2.12}$$

where matrices **A**, **B**, **A** and **D** are presented in Equation (2.11) and contain only constant gains, matrices **U**(s), **X**(s) and **Y**(s) contain Laplace transformation of input variables, state variables as well as output variables, respectively.

A two by three matrix that indicates the input-to-output behavior (i.e., the injections into the input variables yield certain responses in the output variables) of the boost converter, named basic transfer matrix **G**, is solved from the frequency-domain linearized state-space Equation (2.13) [26, p. 20].

$$\mathbf{Y}(s) = [\mathbf{C}(s\mathbf{I} - \mathbf{A})^{-1}\mathbf{B} + \mathbf{D}]\mathbf{U}(s) = \mathbf{G}\mathbf{U}(s) \tag{2.13}$$

Where **I** denotes the identity matrix which has the same order as the system.

$\mathbf{G}(s)$, as presented in Equation (2.14) and (2.15), includes six transfer functions of Laplace variable s, each of them tells how an output signal is affected by a specific sinusoidal input single

when its frequency changes. Hence, transfer functions in $\mathbf{G}(s)$ are solved and named by their physical interpretation.

$$\begin{bmatrix} \hat{i}_{in} \\ \\ \hat{v}_o \end{bmatrix} = \mathbf{G} \begin{bmatrix} \hat{v}_{in} \\ \\ \hat{i}_o \\ \\ \hat{d} \end{bmatrix} = \begin{bmatrix} Y_{in-o} & T_{oi-o} & G_{ci-o} \\ \\ G_{io-o} & -Z_{o-o} & G_{co-o} \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \\ \\ \hat{i}_o \\ \\ \hat{d} \end{bmatrix} \tag{2.14}$$

where

$$\begin{bmatrix} Y_{in-o} & T_{oi-o} & G_{ci-o} \\ \\ G_{io-o} & -Z_{o-o} & G_{co-o} \end{bmatrix} = \frac{\begin{bmatrix} \frac{s}{L} & \frac{D^{'}(1+sr_CC)}{LC} & \frac{V_1(s+\frac{I_o}{V_1C})}{L} \\ \frac{D^{'}(1+sr_CC)}{LC} & -\frac{(r_1-D^{'^2}r_C+sL)(1+sr_CC)}{LC} & \frac{I_o}{D^{'}LC}(\frac{D^{'^2}V_1}{I_o}-r_1-sL)(1+sr_CC) \end{bmatrix}}{(s^2+s\frac{r_1}{L}+\frac{D^{'^2}}{LC})} \tag{2.15}$$

The physical interpretation of each transfer function is expressed below:

1. $\mathbf{G}_{11}(s) = \frac{\hat{i}_{in}}{\hat{v}_{in}}$: Converter input admittance Y_{in-o} (or input impedance Z_{in-o});
2. $\mathbf{G}_{12}(s) = \frac{\hat{i}_{in}}{\hat{i}_o}$: Reverse transfer function T_{oi-o};
3. $\mathbf{G}_{13}(s) = \frac{\hat{i}_{in}}{\hat{d}}$: Control-to-input transfer function G_{ci-o};
4. $\mathbf{G}_{21}(s) = \frac{\hat{v}_o}{\hat{v}_{in}}$: Forward transfer function G_{io-o};
5. $\mathbf{G}_{22}(s) = \frac{\hat{v}_o}{\hat{i}_o}$: Output impedance $-Z_{o-o}$. The sign of $\mathbf{G}_{22}(s)$ is negative because the direction of the output current is opposite to the typical definition for the two-port networks [29, p. 30];
6. $\mathbf{G}_{23}(s) = \frac{\hat{v}_o}{\hat{d}}$: Control-to-output transfer function G_{co-o}.

This kind of input-to-output transfer functions can be further utilized in control design to achieve stable operation of the switching converter.

Similarly, the input-to-state transfer functions are presented as $\mathbf{G}_{state}$ in Equation 2.18, which can be computed from Equation 2.16 and represents the input-to-output behavior.

$$\mathbf{X}(s) = (s\mathbf{I} - \mathbf{A})^{-1}\mathbf{B}\mathbf{U}(s) = \mathbf{G}_{state}\mathbf{U}(s) \tag{2.16}$$

Which can be demonstrated also in the matrix form by specifying the input and state variables:

$$\begin{bmatrix} \hat{i}_L \\ \\ \hat{v}_c \end{bmatrix} = \mathbf{G}_{state} \begin{bmatrix} \hat{v}_{in} \\ \\ \hat{i}_o \\ \\ \hat{d} \end{bmatrix} = \begin{bmatrix} Y_{inL-o} & G_{iL-o} & G_{cL-o} \\ \\ G_{ic-o} & Z_{c-o} & G_{cc-o} \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \\ \\ \hat{i}_o \\ \\ \hat{d} \end{bmatrix} \tag{2.17}$$

where

$$\begin{bmatrix} Y_{inL-o} & G_{iL-o} & G_{cL-o} \\ \\ G_{ic-o} & Z_{c-o} & G_{cc-o} \end{bmatrix} = \frac{\begin{bmatrix} Cs & D^{'} + (CD^{'}r_C s) & I_o + CV_1 s \\ D^{'} & D^{'2}r_C - r_1 - Ls & D^{'}V_1 - \dfrac{I_o(r_1 + Ls)}{D^{'}} \end{bmatrix}}{(D^{'2} + CLs^2 + Cr_1 s)} \tag{2.18}$$

The generalized form of the set of special transfer functions are shown below, which contains the ideal transfer functions, denoted by $G_{ij-\infty}$, which determines the behavior of the corresponding transfer functions at closed loop in low-frequency region [29, p. 143].

$$\begin{bmatrix} Y_{in-sco} & Y_{in-\infty} & T_{oi-\infty} \\ \\ Z^o_{o-oci} & -Z_{o-\infty} & G_{io-\infty} \end{bmatrix} = \begin{bmatrix} Y_{in-o} + \dfrac{G_{io-o}T_{oi-o}}{Z_{o-o}} & Y_{in-o} - \dfrac{G_{io-o}G_{ci-o}}{G_{co-o}} & T_{oi-o} + \dfrac{Z_{o-o}G_{ci-o}}{G_{co-o}} \\ \\ Z_{o-o} + \dfrac{G_{io-o}T_{oi-o}}{Y_{in-o}} & Z_{o-o} + \dfrac{T_{oi-o}G_{co-o}}{G_{ci-o}} & G_{io-o} - \dfrac{Y_{in-o}G_{co-o}}{G_{ci-o}} \end{bmatrix} \tag{2.19}$$

By employing the general form of the special transfer function (Equation 2.19) on the basis of Equation (2.15), Equation 2.20 shows the solved special transfer functions [29, p. 143].

$$\begin{bmatrix} Y_{in-sco} & Y_{in-\infty} & T_{oi-\infty} \\ \\ Z^o_{o-oci} & -Z_{o-\infty} & G_{io-\infty} \end{bmatrix} = \begin{bmatrix} \dfrac{1}{sL + r_1 - D^{'2}r_C} & \dfrac{1}{sL + r_1 - (D^{'2}\dfrac{V_1}{I_o})} & \dfrac{D^{'}(r_C - (\dfrac{V_1}{I_o}))}{sL + r_1 - (D^{'2}\dfrac{V_1}{I_o})} \\ \\ \dfrac{1 + sr_C C}{sC} & \dfrac{(V_1 - r_C I_o)(1 + sr_C C)}{D^{'}V_1(sC + \dfrac{I_o}{V_1})} & \dfrac{I_o(1 + sr_C C)}{D^{'}V_1(sC + \dfrac{I_o}{V_1})} \end{bmatrix} \tag{2.20}$$

where Z^o_{o-oci} is the open-circuit output impedance, which has different value at closed loop because Z_{o-oci} is determined by the state of output voltage feedback. On the contrary, the short-circuit input admittance (Y_{in-sco}) and ideal transfer functions ($G_{ij-\infty}$) are invariant to the state of feedback [29, p. 148].

2.2.5 G-parameter-two-port Model and Control-Block Diagrams

Based on the mathematical models above, the block diagram can be drawn to visualize the dynamics model and to show the mathematical relationships in graphical form [7, p. 24].

Specifically, based on the transfer function matrix at open loop 2.14, the G-parameter-two-port model that represents the small-signal properties is illustrated in Figure 2.5, where its input port is described with Norton's equivalent current source and Thevenin's equivalent voltage source represented its output port [11]. The control block diagrams is demonstrated in Figure 2.6, it represents the open loop input and output dynamics of the boost converter.

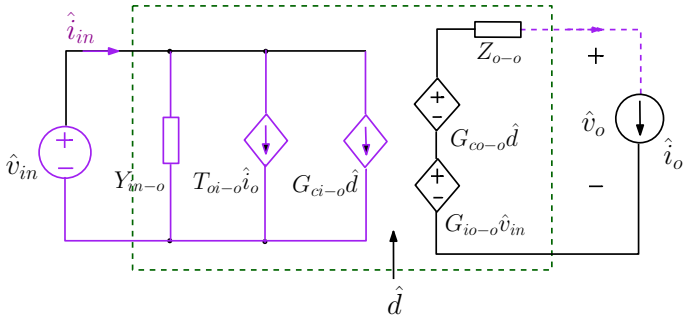
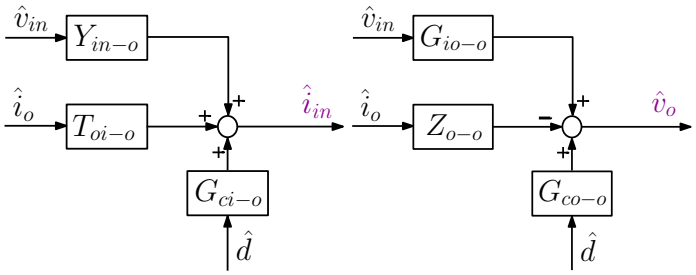


Figure 2.5. *G parameter two-port model of boost converter*



(a) *Input Dynamics* ***(b)*** *Output Dynamics*

Figure 2.6. *Control block diagram of the boost converter at open loop*

The open loop dynamics for input and output port of the converter are constructed according to Figure 2.6:

$$\begin{aligned} \hat{i_{in}} &= Y_{in-o}\hat{v_{in}} + T_{oi-o}\hat{i}_o + G_{ci-o}\hat{d} \\ \hat{v_o} &= G_{io-o}\hat{v_{in}} - Z_{o-o}\hat{i}_o + G_{co-o}\hat{d} \end{aligned} \tag{2.21}$$

2.3 System Dynamic Response

This section introduces the fundamentals of the frequency response depicted by bode plots for estimating the stability of a system, and the time-domain step response that reflects the characteristics of the system.

2.3.1 Frequency Response

The frequency response is the linear system output caused by a sinusoidal input, it reveals how the system output response to the input in the Fourier Domain [7, p. 315]. Figure 2.7 displays the basic principle of the frequency response in an LTI system. In this figure, the system input is represented by $X_{in} = M_i \sin(\omega t + \phi_i)$ where M_i and ϕ_i is the input magnitude and input phase, respectively. The system output is represented by $Y_{out} = X_{in}\mathbf{G}(s) = M_o \sin(\omega t + \phi_o)$, where M_o and ϕ_o is the output magnitude and output phase, respectively. $\mathbf{G}(s)$ denotes the input-to-output transfer function of a linear time-invariant (LTI) system.

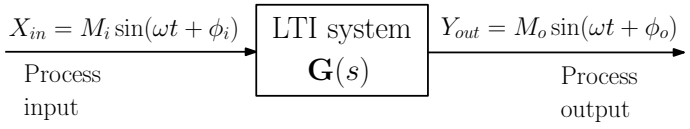


Figure 2.7. *Basic principle of the frequency response in an LTI system*

This figure means that if an LTI system has a sinusoidal input at angular frequency ω with

magnitude M_i and phase ϕ_i, the system output computed from the transfer function $\mathbf{G}(s)$ will be sinusoidal at the same frequency ω, but with changed magnitude M_o and phase ϕ_o [7, p. 100]. The magnitude response ($\mid \mathbf{G}(j\omega) \mid$) and phase response ($\angle\mathbf{G}(j\omega)$) are defined as:

$$\begin{aligned} \mid \mathbf{G}(j\omega) \mid &= \frac{M_o}{M_i} \\ \angle\mathbf{G}(j\omega) &= \phi_o - \phi_i \end{aligned} \tag{2.22}$$

Frequency response of transfer functions are often analyzed by plotting the Bode plot, where the corresponding system response is drawn for each frequency point. Bode plot is a critical tool for designing the dynamic compensator. The phase and magnitude of a transfer function are normally expressed in degrees ($^\circ$) and decibel (dB) in the Bode plot, respectively [29, p. 77].

2.3.2 Poles and Zeros

A basic tool for performing a transfer function mathematically is called partial-fraction expansion that represents $\mathbf{G}(s)$ as a ratio of two polynomials with regards to s (Laplace variable) [7, p. 109]:

$$\mathbf{G}(s) = \frac{b_1 s^m + b_2 s^{m-1} + \cdots + b_{m+1}}{s^n + a_1 s^{n-1} + \cdots + a_n} \tag{2.23}$$

which can also be displayed in terms of the product of factors as:

$$\mathbf{G}(s) = K\frac{(s+\omega_{z1})(s+\omega_{z2})\cdots(s+\omega_{zm})}{(s+\omega_{p1})(s+\omega_{p2})\cdots(s+\omega_{pn})} \tag{2.24}$$

Zeros (ω_{zi}) and poles (ω_{pi}) correspond to the roots of the numerator polynomial and denominator polynomial, respectively [29, p. 77].

The zeros represent the signal transmission-blocking properties of the system, which means if a nonzero input is excited to the system, the system output is identically zero for frequencies where $s_0 = \omega_{zi}$ and $s_0 \neq \omega_{pi}$ [7, p. 115]. Whereas the system stability properties are mainly determined by the poles [7, p. 115].

Dominant zeros and poles are the roots that positioned closest to the origin of s-plane, which have the greatest impact on the transient response of the corresponding system. Consequently, the location of the zeros and poles should be recognized for the purpose of apprehending the influence of diverse transfer functions on the system dynamic behaviors. [29, p. 77]

2.3.3 Effect of Locations of Poles and Zeros on System Dynamics

Generally, the zeros and poles are the numbers on the complex plane, i.e, $s = \alpha + j\beta$, and pole-zero map is a useful tool to display the system dynamics graphically, it plots the positions of poles and zeros on the complex-plane. The system characteristics of the transient performance can be estimated by the location of zeros and poles, and further, affect the control system design.

Normally, the LHP-zero introduces damping to a step response, which prevents the system from unstable. More specifically, an LHP zero is able to raise the overshoot, reduce the peak time as well as the rise time, which means the frequency response will be faster under the effect of a LHP zero [7, p. 140-147]. However, it does not have a notable influence on the settling time.

An RHP zero, also called nonminimum-phase zero, will depress the overshoot, slow down the system, and perhaps lead the step response to the wrong direction [7, p. 147]. From the perspective of the Bode plot, the RHP zero will raise the loop gain and reduce the loop phase, which is more demanding to the control design because the corresponding converter is more likely to show instability [26, p. 50].

Mapping from the pole-zero map to time-domain performance obtained through inverse Laplace transformation as displayed in Figure 2.8, it can be observed that the real part (α) generally introduces damping behavior and imaginary part (β) introduces oscillation behaviors to a step re-

sponse. Therefore, the position of the poles in the s-plane decides the system dynamic behaviors as presented below [7, p. 129]:

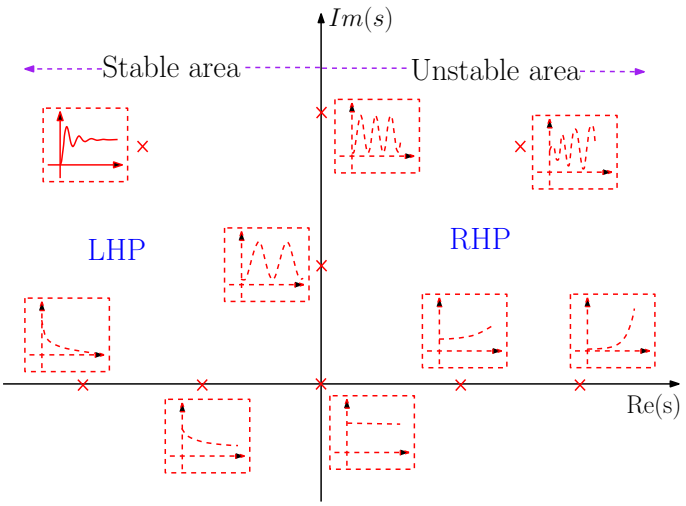


Figure 2.8. *Time functions associated with the location of the poles in the complex-plane*

1. A real negative pole lies in the LHP ($p_i = -\alpha$) corresponds to $Ce^{-\alpha t}$ in time-domain, which generates an exponential component that is decaying. The pole location determines the rate of decay in a way that the farther the poles away from the origin in the LHP, the more rapid the exponential component decay, and vice versa.

2. A conjugate pole pair in the LHP ($s = -\alpha \pm j\beta$) corresponds to $Ae^{-\alpha t}\sin(\omega t + \phi)$ in time-domain, where A and ϕ are specified by the initial state. This function generates a response that is decaying in a sinusoidal form. The decay rate is determined by α while the oscillation frequency is specified by ω.

3. A pole locates at the origin ($p_i = 0$) defines a constant component whose amplitude is defined by the initial state.

4. A pole pair that located on the imaginary axis ($s = \pm j\beta$) defines an oscillatory component whose amplitude is constant and it is determined by the initial settings, this kind of system is defined as marginally stable.

5. A real positive pole in the RHP ($p_i = +\alpha$) corresponds to $Ce^{\alpha t}$ in time-domain, which defines an exponentially increasing component, thus the system will be unstable.

6. A pole pair in the RHP ($s = +\alpha \pm j\beta$) corresponds to $Ae^{\alpha t}\sin(\omega t + \phi)$ in time-domain, where A and ϕ are specified by the initial settings. This function generates an exponentially increasing component which is unstable.

Based on the above information, RHP poles normally make systems unstable, because the imaginary pole-pairs will create unwanted distortion in the system response, and this oscillation will be amplified if the pole has a positive real part [7]. In this case, the distortion in an unstable system need to be damped by a proper control design. On the contrary, systems with LHP poles are stable in general.

2.3.4 Transfer Functions of Second-Order System

Many resonant systems are capable to be approximated using a second-order system transfer function, which is typically expressed as:

$$\mathbf{G}(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{2.25}$$

where ζ is known as the damping ratio while ω_n denotes the undamped natural frequency. Damping ratio determines how much oscillation will be present in the system. A system with a small damping ratio has a large overshoot, nevertheless, it also means small rise time [5].

Step response is introduced as an example to help us better understand the effect of the system characteristics on transient performance. Assume that a unit step is made at the input of the system, which can be expressed as $U(s) = \frac{1}{s}$ in frequency-domain. Then the output of the system in frequency-domain through this second-order transfer function would be given as:

$$\mathbf{Y}(s) = \frac{\omega_n^2}{s(s^2 + 2\zeta\omega_n s + \omega_n^2)} \tag{2.26}$$

The step response in time-domain (also called transient performance or transient response) is a unit step with exponentially sinusoidal component either decaying (in a stable system) or increasing oscillation (in an unstable system). It can be acquired by applying the inverse Laplace transformation on the system output $\mathbf{Y}(s)$, yields:

$$y(t) = 1 - \frac{1}{\sqrt{1-\zeta^2}} e^{-\zeta\omega_n t} \sin(\omega_d t + \phi) \tag{2.27}$$

where the damped natural frequency is $\omega_d = \omega_n\sqrt{\zeta^2 - 1}$, phase $\phi = \arctan(\frac{\sqrt{1-\zeta^2}}{\zeta})$.

2.3.5 Link between Transfer Functions and Time-domain Properties

In the case of the switched-mode DC-DC boost converter, its transfer functions have been solved in Equation 2.15, the common denominator of the transfer functions $(s^2 + s\frac{r_1}{L} + \frac{D^{'2}}{LC})$ has close resemblance to the second-order transfer function $(s^2 + 2\zeta\omega_n s + \omega_n^2)$. In other words, the transfer functions of a boost converter is approximated as a second-order system. Therefore, the system characteristics of the boost converter in transient response can be obtained as below [29, p. 149]:

$$\begin{aligned}
&\text{Undamped natural frequency: } \omega_n = \frac{D^{'}}{\sqrt{LC}} \\
&\text{Damped nutural frequency: } \omega_d = \frac{D^{'}}{\sqrt{LC}}\sqrt{1 - (\frac{r_1}{2D^{'}}\sqrt{\frac{C}{L}})^2} \\
&\text{Damping ratio: } \zeta = \frac{r_1}{2D^{'}}\sqrt{\frac{C}{L}} \\
&\text{Quality factor: } Q = \frac{D^{'}}{r_1}\sqrt{\frac{L}{C}}
\end{aligned} \tag{2.28}$$

It is notable that ζ and ω_n change with the steady-state operating point.

2.4 Impedance-Based Stability Assessment

The basic idea of impedance-based stability assessment is presented in this section. It is mainly founded on the impedance ratio determination and NSC.

2.4.1 Nyquist Stability Criterion

NSC is developed on the basis of the argument principle, is a helpful tool for judging the system stability based on its frequency response [7, p. 338].

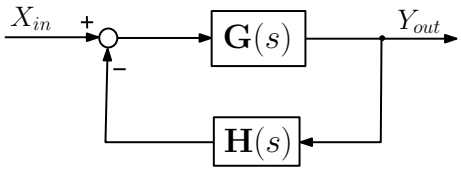


Figure 2.9. *Block diagram for a simple feedback control system*

To apply NSC to the feedback control design, assume system at closed loop as given in Figure 2.9, where $H(s)$ denotes the feedback transfer function, $G(s)$ is the transfer function that describes open loop state. The control loop gain is established as $L(s) = G(s)H(s)$. Accordingly, the transfer function at closed loop is expressed as:

$$\frac{Y(s)}{X(s)} = \frac{G(s)}{1 + L(s)}$$

As presented in the last section, a system is unstable when RHP poles are included in its transfer function. Thus, with the purpose of determining the system stability, the poles solved from the transfer function at closed loop (i.e., zeros of denominator term $1 + L(s)$) should be analyzed.

According to the argument principle to the function $1 + L(s)$, assuming the loop gain $L(s)$ does not contain RHP pole, an encirclement of -1 by $L(s)$ implies a RHP zero of $1 + L(s)$. The key principle of the Nyquist Stability Criterion is $Z = N + P$, where Z equals the number of RHP-zeros (i.e., roots of closed loop system), N denotes the net number of clockwise encirclements, P is the number of open loop RHP-poles [7, p. 341]. In other words, a feedback system is seen to be stable if and only if the outline of the loop gain $L(s)$ in the imaginary plane does not encircle $(-1, j0)$ point, when there is no RHP-pole exists [14].

2.4.2 Gain Margin and Phase Margin

Nyquist diagram, also named polar plot or Nyquist plot, is a widely utilized tool for identifying the stability of feedback systems. The Nyquist diagram of the whole transfer function is constructed by computing its phase and magnitude at different frequencies along the j-axis [3]. Phase margin (PM) together with Gain margin (GM) are two commonly used signs on a Nyquist plot to investigate the stability properties of a system, as illustrated in Figure 2.10.

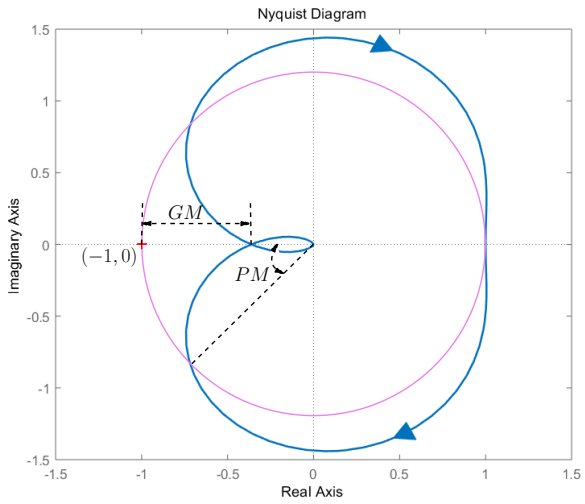


Figure 2.10. *Nyquist plot for defining Phase margin and Gain margin*

Gain margin defines how much the magnitude of the loop gain has to increase until the Nyquist diagram encircles the $(-1, j0)$ point. If we measure the GM on the Bode plot, it displays how much

the loop gain magnitude needs to rise before the negative feedback turns into positive feedback [4]. Generally, a system with a larger gain margin is more stable.

Phase margin defines how much the phase of the loop gain needs to drop before the system becomes unstable. The system is more relatively stable with a larger phase margin in general. Normally, an adequate PM ($PM > 45°$) should be guaranteed to prevent the system to become unstable.

The PM and GM could be obtained from the Bode plot at well, as illustrated in Figure 2.11. The frequency that corresponds to a unity magnitude is defined as the gain crossover frequency ω_{gco}. Similarly, the frequency that corresponds to the phase value of $-180°$ is defined as phase crossover frequencies ω_{phco}. [29, p. 89].

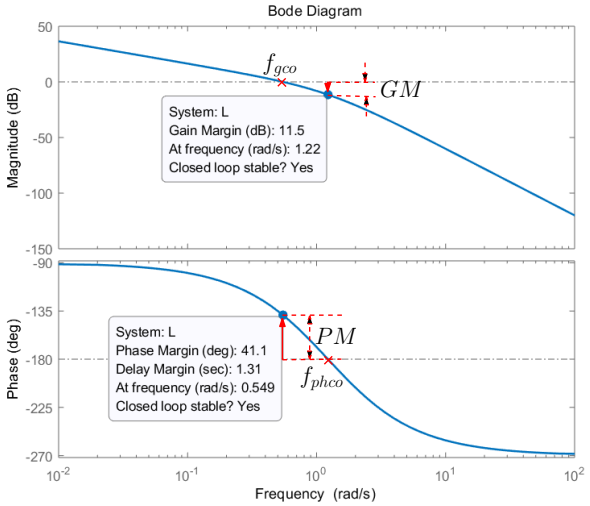


Figure 2.11. *Bode plot for defining Gain margin and Phase margin*

2.4.3 Impedance-Based Stability Assessment

The impedance-based stability assessment approach is widely used to access the transient response and stability of power electronic systems [29, p. 92]. The first application of this assessment dates from 1976 by Middlebrook, which yielded the design rule of the input EMI filter of DC-DC converters to prevent the input EMI filters from affecting the converter dynamics and causing instability through its output impedance [18]. The impedance-based stability method decomposes the whole system into a load and a source subsystem at a given point of common connection, providing an attractive way for analyzing the stability of cascade-connected systems [23]. The system stability is guaranteed if the impedance-ratio (also termed minor loop gain) meets the NSC, where the impedance ratio is constructed as the ratio of the output impedance of input EMI filter and the input impedance of the boost converter at closed loop [26, p. 6]. Small-signal modeling can be used to perform such a stability analysis by introducing a small perturbation into the system.

This impedance-based stability method is flexible to use because it only considers the frequency response of the impedances of the divided subsystems at the terminal without knowing the internal parameters [23]. Another reason that the impedance-based method is preferred in this thesis is that the system stability can be easily assessed from simulations in the system with respect to a single point.

3 DYNAMIC MODELING IN DIFFERENT CONTROL MODE

In Chapter 2, the transfer functions of boost converter at open loop are derived and the basics of system response, the impedance-based stability criterion are also introduced. Actually, open loop switched-mode converters are unable to regulate and maintain their output as expected without proper control. Moreover, the controller plays an essential role in overcoming the non-linearity of the system due to switching actions [2].

This chapter introduces the physical implementation and the duty ratio generation process of two control techniques applied in switched-mode converters briefly. With knowing the control techniques, the dynamic modeling of the voltage-fed boost converter under both Average-Current-Mode (ACM) control and Direct-Duty-Ratio (DDR) control are presented.

3.1 Control Techniques Utilized in Switched-mode Converters

This section presents the basic structure and working principle of two frequently used control modes, i.e., CMC and DDR method. The control mode is defined by the way of producing the length of On-time (T_{on}) [29, p. 56]. T_{on} is generated with reference to the constant-slope ramp signal in VMC while this signal is produced using the instantaneous inductor current in CMC [29, p. 56]. Then, peak-current-mode (PCM) control as well as average-current-mode (ACM) control techniques are introduced further.

3.1.1 Direct-Duty-Ratio Control of Switched-mode Converters

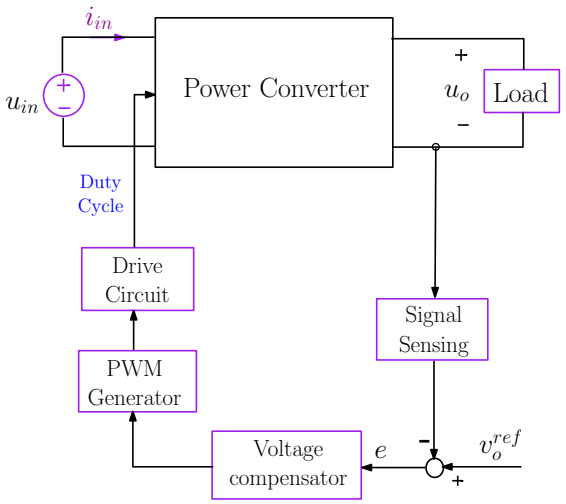


Figure 3.1. *Basic structure of the Direct-Duty-Ratio control*

Figure 3.1 displays the fundamental structure of Direct-On-Time (DOT) control (also known as DDR control when the switching frequency f_s is fixed). It is a controller with a single loop that compares the measured output voltage v_o to a reference voltage V_o^{ref}, the generated error e is

compensated by the voltage compensator and its output value v_c is used as the control signal that determines the duty ratio of the transistor [12]. This duty ratio $d = \frac{t_{on}}{T_s}$, which is utilized as the control variable, helps the output voltage reach the predefined level and maintain constant. It is produced by the pulse width modulator (PWM) by comparing v_c to a constant-slope PWM signal ($M_{PWM} = \frac{V_M}{T_s}t$) [29, p. 128].

It is notable that the slope of the PWM ramp affects the dynamic actions of the converter via the modulator. This effect is evaluated via the modulator gain G_{PWM} which usually equals $\frac{1}{V_M}$, where V_M is the amplitude of the waveform in PWM [29, p. 128].

VMC method is used in view of the fact that it is not only easy to implement, but also provides immunity against disturbances in the input signal. However, there are several disadvantages of this control method, such as poor reliability, slow response as well as poor performance in complex systems. [2]

3.1.2 Current Mode Control of Switched-mode DC-DC Converters

CMC is constructed in such a manner that a voltage and a current control loop form a dual-loop controller as illustrated in Figure 3.2. At first, the difference between the sensed output voltage and the voltage reference value is the error signal, also known as the control signal. It is utilized as the reference value of i_L. Similarly, the measured inductor current, as a feedback state, is compared to this control signal to give the switching duty ratio. It is notable that the inner inductor current control loop is required to be faster than the output voltage loop because the inductor current should be able to track its reference faster than the output voltage loop can change it.

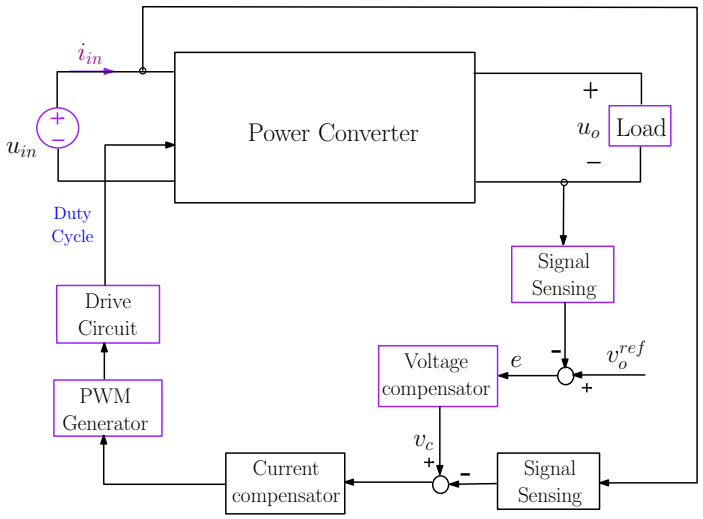


Figure 3.2. *Basic structure of the Current Mode Control*

Although it may cause sub-harmonic oscillation to the system, the CMC method has many merits, such as higher sensitivity to the changing of input voltage, high reliability, as well as providing short-circuit and overload protections [2]. Among CMC methods, ACM control and PCM control are two approaches that are mostly used.

In the PCM control, the measured inductor current is compared to a control input, the transistor switch is switched off once the peak inductor current reaches the control value. This working principle gives inherent over-current protection to the PCM method. However, PCM is susceptible to noise as the current ramp is normally pretty small in comparison with the control signal level. Thus, slope compensation is required to eliminate sub-harmonic oscillations and ensure proper operation.

On the other side, in ACM controller, the average inductor current is compared to the control

signal and is controlled to follow the reference values. ACM control has a slower dynamic response than PCM control, nevertheless, this technique is mainly preferred due to its better noise immunity and it can be used in applications that require high accuracy of current regulation [31].

Considering the above points, the ACM control method is utilized in this case.

3.2 Dynamic Models of DDR-controlled DC-DC Boost Converter

The small-signal modeling of the DDR-controlled VF DC-DC boost converter operates in CCM is provided in this section, which is the basis of the dynamic models under ACM control.

3.2.1 Circuit Schematics of DC-DC Boost Converter Under DDR control

Figure 3.3 depicts the circuit schematics of a boost converter under DDR control. The sensed converter output voltage is in comparison with the voltage reference value in the error amplifier to yield a control voltage, then this control signal is connected to the PWM to drive the MOSFET.

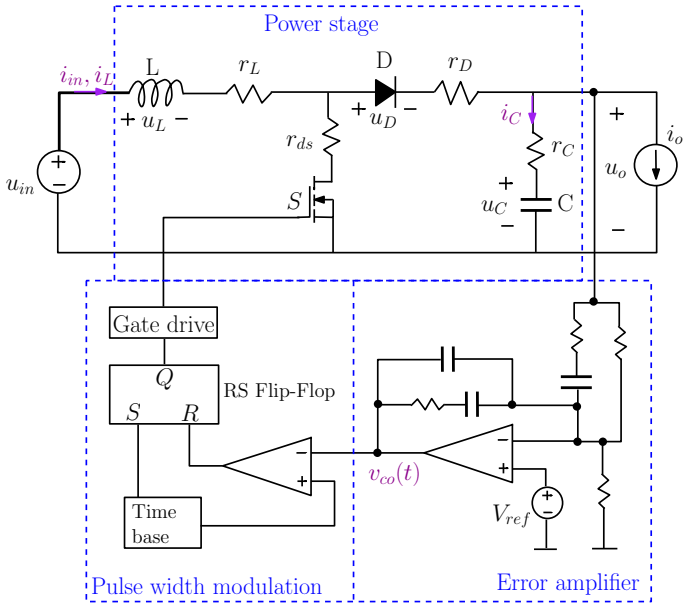


Figure 3.3. *Circuit schematics of boost converter under Direct-duty-ratio control*

The voltage-mode-control equals to DDR control when f_s is constant, where the duty ratio is given as $d = \frac{t_{on}}{T_s}$ and cycle time T_s is defined by the inverse of the switching frequency f_s. In the pulse-width generation process of DDR control, the aforementioned control voltage is in comparison with a constant-slope sawtooth ramp. The duty cycle is changed with the control signal caused by the varying converter output voltage, which in turn adjusts the output voltage to follow its reference signal. The duty cycle generation managed by the control signal v_{co} is shown in Figure 3.4.

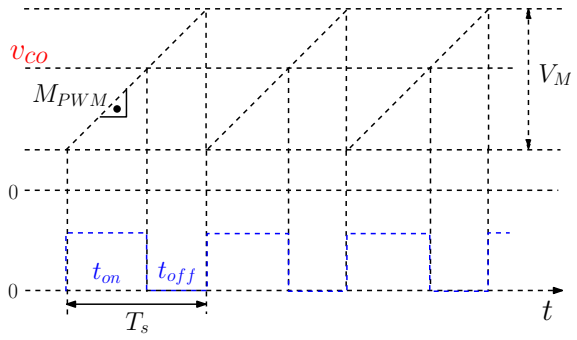


Figure 3.4. *Pulse-width generation of boost converter under Direct-duty-ratio control*

Based on Figure 3.4, the control signal can be expressed as:

$$v_{co} = \frac{V_M}{T_s} t_{on}$$

By linearizing the expression of v_{co}, yields the duty ratio under DDR control:

$$\hat{d} = \frac{1}{V_M} \hat{v}_{co}$$

3.2.2 Dynamic Models of DDR-Controlled Boost Converter at Open loop

Figure 3.5 illustrates the power stage of the DDR-controlled boost converter with a PWM modulator. The PWM gain is assumed to be unity, the source impedance (Z_S) is assumed to be infinite while the load admittance (Y_L) is assumed to be zero when constructing the internal dynamic model of the DDR-controlled boost converter at open loop [29, p. 129].

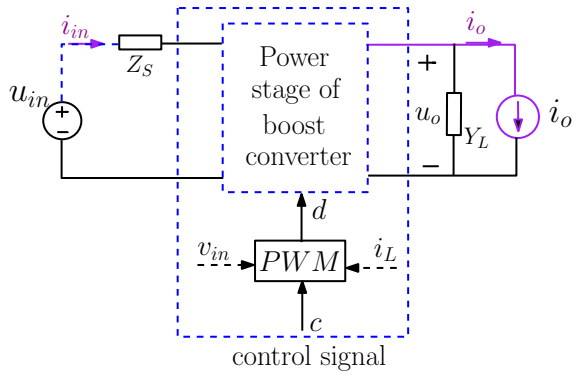


Figure 3.5. *DDR-controlled boost converter at open loop with a PWM*

A converter is considered to be working at closed loop only if the feedback loop from the targeted output variable is connected, otherwise, it works at open loop in terms of the final control even it contains internal feedback [29]. Thus, the power stage of the PWM modulated boost converter can be viewed as an open loop, since the output voltage feedback is not connected.

According to the SSA method introduced in Chapter 2, the general state-space for the switched-

mode DC-DC boost converter under DDR-control at open loop is provided as:

$$\begin{aligned}\frac{d\langle i_L\rangle}{dt} &= \frac{t_{on}}{t_s}m_1 - \frac{t_{off}}{t_s}m_2\\ \frac{d\langle v_C\rangle}{dt} &= \frac{t_{off}}{t_{on}+t_{off}}\frac{\langle i_L\rangle}{C} - \frac{\langle i_o\rangle}{C}\\ \langle i_{in}\rangle &= \langle i_L\rangle\\ \langle v_o\rangle &= \langle v_C\rangle - r_C C\frac{d\langle v_C\rangle}{dt}\end{aligned} \tag{3.1}$$

where the up-slope (m_1) and down-slope (m_2) are given below:

$$\begin{aligned}m_1 &= \frac{\langle V_{in}\rangle - (r_L + r_{ds})\langle i_L\rangle}{L}\\ m_2 &= \frac{(r_L + r_D + r_C)\langle i_L\rangle + \langle v_C\rangle - r_C\langle i_o\rangle + V_D - \langle v_{in}\rangle}{L}\end{aligned} \tag{3.2}$$

By implementing the transformation between the general state-space and frequency-domain (i.e., Laplace domain), then applying the linearization techniques on the basis of Equation 3.1, yields the transfer function matrix of DDR-controlled boost converter at open loop:

$$\begin{bmatrix}\hat{i}_{in}\\ \hat{v}_o\end{bmatrix} = \begin{bmatrix}Y_{in-o}^{DDR} & T_{oi-o}^{DDR} & G_{ci-o}^{DDR}\\ G_{io-o}^{DDR} & -Z_{o-o}^{DDR} & G_{co-o}^{DDR}\end{bmatrix}\begin{bmatrix}\hat{v}_{in}\\ \hat{i}_o\\ \hat{d}\end{bmatrix} \tag{3.3}$$

where

$$\begin{bmatrix}Y_{in-o}^{DDR} & T_{oi-o}^{DDR} & G_{ci-o}^{DDR}\\ G_{io-o}^{DDR} & -Z_{o-o}^{DDR} & G_{co-o}^{DDR}\end{bmatrix} = \frac{\begin{bmatrix}\frac{s}{L} & \frac{D^{'}(1+sr_CC)}{LC} & \frac{V_1(s+\frac{I_o}{V_1C})}{L}\\ \frac{D^{'}(1+sr_CC)}{LC} & -\frac{(r_1 - D^{'2}r_C + sL)(1+sr_CC)}{LC} & \frac{I_o}{D^{'}LC}(\frac{D^{'2}V_1}{I_o} - r_1 - sL)(1+sr_CC)\end{bmatrix}}{(s^2 + s\frac{r_1}{L} + \frac{D^{'2}}{LC})} \tag{3.4}$$

As introduced in Chapter 2, the input-to-state transfer functions under DDR control at open loop are presented as:

$$\begin{bmatrix}\hat{i}_L\\ \hat{v}_c\end{bmatrix} = \begin{bmatrix}Y_{inL-o}^{DDR} & G_{iL-o}^{DDR} & G_{cL-o}^{DDR}\\ G_{ic-o}^{DDR} & Z_{c-o}^{DDR} & G_{cc-o}^{DDR}\end{bmatrix}\begin{bmatrix}\hat{v}_{in}\\ \hat{i}_o\\ \hat{d}\end{bmatrix} \tag{3.5}$$

where

$$\begin{bmatrix}Y_{inL-o}^{DDR} & G_{iL-o}^{DDR} & G_{cL-o}^{DDR}\\ G_{ic-o}^{DDR} & Z_{c-o}^{DDR} & G_{cc-o}^{DDR}\end{bmatrix} = \frac{\begin{bmatrix}Cs & D^{'} + (CD^{'}r_Cs) & I_o + CV_1s\\ D^{'} & D^{'2}r_C - r_1 - Ls & D^{'}V_1 - \frac{I_o(r_1+Ls)}{D^{'}}\end{bmatrix}}{(D^{'2} + CLs^2 + Cr_1s)} \tag{3.6}$$

3.2.3 Definition of Loop Gain

Loop gain is used as a critical means of investigating the system stability, it reflects how the signal at the output side is fed back to the input side around a feedback loop [9]. By imagining the feedback loop is broken at an arbitrary point as displayed in Figure 3.2.3, the control loop gain can be defined as below.

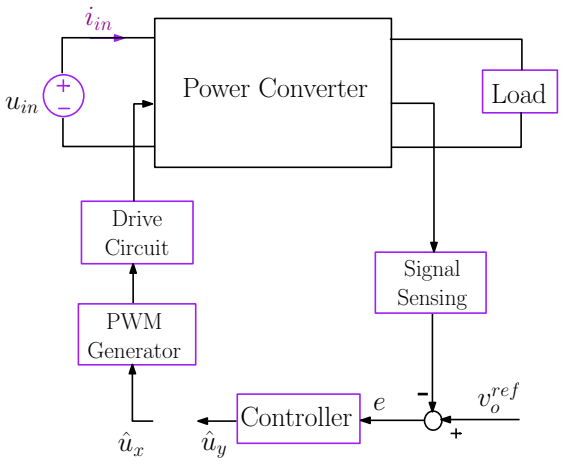


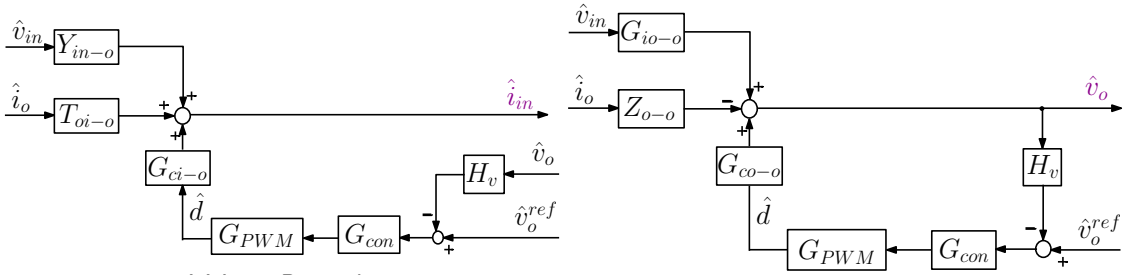
Figure 3.6. *Definition of loop gain*

$$L(s) = -\frac{\hat{u}_y(s)}{\hat{u}_x(s)}$$

In practice, the transfer function of the control loop gain can be acquired by solving the open loop dynamic model of the converter in the frequency-domain and adding the Laplace-transformed versions of sensing, controller and PWM functions. Generally, the corresponding transfer function at open loop can be given by the dynamic models. Sensing transfer function ($H(s)$) normally depends on the physical implementation. The controller transfer function ($G_{con}(s)$) is known because it is a design problem that is solved artificially. PWM may introduce gain (G_{PWM}) and delay (G_{del}) depending on its implementation. Additionally, the digital control system also introduces delay and sampling effect. [29]

3.2.4 Control Block Diagram of DDR-Controlled Boost Converter

Founded on the basic open loop transfer functions derived in Equation 3.4 as well as the voltage mode control structure, the control block diagram of the DDR-controlled boost converter at closed loop is illustrated in Figure 3.7, where the feedback from output voltage is applied.



(a) *Input Dynamics*

(b) *Output Dynamics*

Figure 3.7. *Control block diagram of the DDR-controlled boost converter at closed loop*

In the case of a DDR-controlled boost converter, to achieve closed loop control, the measured output voltage is in comparison with the reference signal v_{ref}. The input of the pulse-width modulator (PWM) comes from the output of the outer voltage loop compensator (G_{con}), and the PWM outputs the duty cycle perturbation $\hat{d}$. The modulator is essential for translating the output signal of the control loop to switching signals that can be recognized by the semiconductor switches of the converter. This modulation process can be easily done by comparing the controller signal to a triangle waveform in a comparator.

Accordingly, the voltage control loop gain L_{DDR} can be identified as the product of all the gains along the feedback loop. In a small-signal model, control-to-input-current transfer function G_{co-o}^{DDR} is solved in Equation 3.4. Then, sensing gain $H_v(s)$ is assumed unity in this case where the controller is designed afterward with Simulink and the transfer function of PWM is simply a gain $\frac{1}{V_M}$. The controller transfer function is G_{con}. The resulted DDR control loop gain is:

$$L_{DDR} = G_{co-o}^{DDR} G_{PWM} G_{con} H_v \tag{3.7}$$

By plotting the frequency response of uncompensated loop gain, where G_{con} is set to 1 in L_{DDR}, the desired crossover frequency and acceptable PM are capable to be resolved according to the shape of the uncompensated bode plots. Accordingly, the loop shaping technique can be applied to shape the voltage loop compensator.

3.2.5 Dynamic Models of DDR-Controlled Boost Converter at Closed-loop

The closed loop input and output dynamics can be determined based on the open loop dynamics in Equation (2.21) by substituting $\hat{d} = G_{PWM} G_{con}(\hat{v}_o^{ref} - H_v \hat{v}_o)$ for the duty ratio [29, p. 129]:

$$\begin{aligned} \hat{i}_{in}^{DDR} &= Y_{in-c}^{DDR} \hat{v}_{in} + T_{oi-c}^{DDR} \hat{i}_o + G_{ci-c}^{DDR} \hat{v}_o^{ref} \\ \hat{v}_o^{DDR} &= G_{io-c}^{DDR} \hat{v}_{in} - Z_{o-c}^{DDR} \hat{i}_o + G_{co-c}^{DDR} \hat{v}_o^{ref} \end{aligned} \tag{3.8}$$

Where

$$\begin{bmatrix} Y_{in-c}^{DDR} & T_{oi-c}^{DDR} & G_{ci-c}^{DDR} \\ G_{io-c}^{DDR} & -Z_{o-c}^{DDR} & G_{co-c}^{DDR} \end{bmatrix} =$$

$$\begin{bmatrix} Y_{in-o} - \dfrac{L_{DDR}}{1+L_{DDR}} \dfrac{G_{ci-o} G_{io-o}}{G_{co-o}} & T_{oi-o} + \dfrac{L_{DDR}}{1+L_{DDR}} \dfrac{G_{ci-o} Z_{o-o}}{G_{co-o}} & \dfrac{G_{ci-o}}{G_{co-o}} \dfrac{L_{DDR}}{H_v(1+L_{DDR})} \\ \dfrac{G_{io-o}}{1+L_{DDR}} & -\dfrac{Z_{o-o}}{1+L_{DDR}} & \dfrac{L_{DDR}}{H_v(1+L_{DDR})} \end{bmatrix}$$

The input and state dynamics for DDR (3.9) can be solved in a similar way, by substituting $\hat{d} = G_{PWM} G_{con}(\hat{v}_o^{ref} - H_v \hat{v}_o^{DDR})$ into the duty ratio of the open loop input and state dynamics, where $\hat{v}_o^{DDR}$ is shown in Equation 3.8:

$$\begin{aligned} \hat{i}_L^{DDR} &= Y_{inL-c}^{DDR} \hat{v}_{in} + G_{iL-c}^{DDR} \hat{i}_o + G_{cL-c}^{DDR} \hat{v}_o^{ref} \\ \hat{v}_C^{DDR} &= G_{iC-c}^{DDR} \hat{v}_{in} + Z_{C-c}^{DDR} \hat{i}_o + G_{cC-c}^{DDR} \hat{v}_o^{ref} \end{aligned} \tag{3.9}$$

Where

$$\begin{bmatrix} Y_{inL-c}^{DDR} & G_{iL-c}^{DDR} & G_{cL-c}^{DDR} \\ G_{iC-c}^{DDR} & Z_{C-c}^{DDR} & G_{cC-c}^{DDR} \end{bmatrix} =$$

$$\begin{bmatrix} Y_{inL-o} - G_{cL-o} H_v G_{io-c}^{DDR} & G_{iL-o} + (G_{cL-o} H_v Z_{o-c}^{DDR}) & G_{cL-o}(G_{PWM} G_{con}^{DDR} - H_v G_{co-o}^{DDR}) \\ G_{iC-o} - G_{cC-o} H_v G_{io-o}^{DDR} & Z_{C-o} + G_{cC-o} H_v Z_{o-c}^{DDR} & G_{cC-o}(G_{PWM} G_{con}^{DDR} - H_v G_{co-o}^{DDR}) \end{bmatrix}$$

3.3 Dynamic Models of ACM-controlled boost converter

This section develops the small-signal model of the ACM-controlled boost converter in CCM on the basis of the DDR dynamic models by making use of the control block diagram. The dynamic models for ACM are mainly obtained by using a proper duty ratio constraint rather than the perturbed duty ratio. This small-signal duty ratio is constructed as a function of related variables of circuit in the generation process of duty ratio [29, p. 189].

3.3.1 Circuit Schematics of Boost Converter Under ACM Control

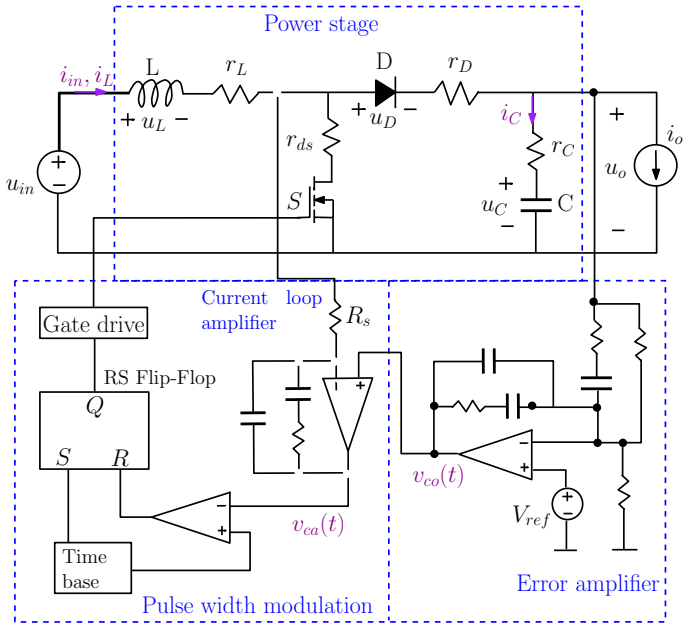


Figure 3.8. *Circuit Schematics of Boost Converter Under ACM control*

As Figure 3.8 shows, the duty ratio is produced by the PWM which compares output signal (v_{ca}) of the inductor current compensator to the ramp signal ($R_s M_c$), where R_s represents the sensing resistor, and M_c denotes the PWM ramp slope [29, p. 225].

The generation process of duty ratio under ACM control is pictured in Figure 3.9. The transistor keeps conducting when the output signal (v_{ca}) is bigger than the PWM ramp signal ($R_s M_c$), and vice versa [29, p. 225]. The expression for v_{ca} can be computed as shown in Equation 3.11.

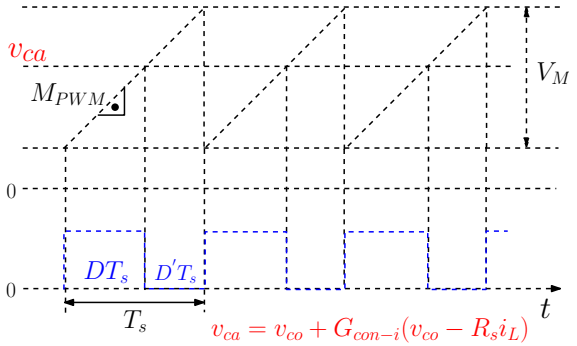


Figure 3.9. *Duty Ratio Generation of Boost Converter Under ACM control*

$$v_{ca} = v_{co} + G_{c-i}(v_{co} - R_s i_L) \tag{3.10}$$

where v_{co} represents the output value of the output voltage controller. i_L denotes the instantaneous inductor current which consists of time-varying average inductor current ($\langle i_L \rangle$) as well as the triangle-shaped ripple current ($i_{L-ripple}$) [29, p. 226]. G_{c-i} is the current compensator transfer function. Thus, v_{ca} can also be given as:

$$v_{ca} = v_{co} + G_{c-i}(v_{co} - R_s\langle i_L \rangle) - G_{c-i}R_s i_{L-ripple} \tag{3.11}$$

The corresponding output signal of the current compensator in current domain can be expressed as [29, p. 226]:

$$i_{ca} = (1 + G_{c-i})\langle i_{co} \rangle - G_{c-i}\langle i_L \rangle - K_f i_{L-ripple} \tag{3.12}$$

where $\langle i_{co} \rangle$ is the average control current value. K_f means the gain of the current loop compensator at f_s which describes the switching ripple in i_L. However, the ripple effect can be ignored under digital control (i.e., $K_f = 0$). [29, p. 226]

3.3.2 Duty Ratio Constraints for ACM Control

Duty ratio constraint is a relation of the dynamic behaviors tied to the duty ratio and on-time when applying the new control approach [29, p. 125]. Typically, duty ratio constraint is expressed as Equation 3.13 [29, p. 189]:

$$\hat{d} = F_m(\hat{x}_C - \sum_{i=1}^{n} q_i \hat{x}_i) \tag{3.13}$$

where x_C is the new control variable and q_i denotes the feedforward or feedback gain of variable x_i. F_m is the duty ratio gain [29, p. 189].

According to the generation process of the duty ratio presented in Figure 3.9 without taking ripple effect into account, the duty ratio constraint for ACM control is given as [29, p. 228]:

$$\hat{d} = G_{PWM} i_{ca} = F_m((1 + G_{c-i})\hat{i}_{co} - G_{c-i}\hat{i}_L) \tag{3.14}$$

where $G_{PWM} = F_m = \dfrac{1}{R_s T_s M_c} = \dfrac{1}{V_M}$, V_M denotes the maximum magnitude value of the PWM ramp [29, p. 228].

3.3.3 Control Block Diagram for Average-Current Mode Control

The control block diagram for the ACM-controlled boost converter at open loop in CCM is illustrated in Figure 3.10, from where we can acquire the dynamic models of the ACM-controlled boost converter in CCM. It represents open loop for ACM control because only the inductor current loop is closed in this control block diagram while the final output voltage feedback is not connected yet.

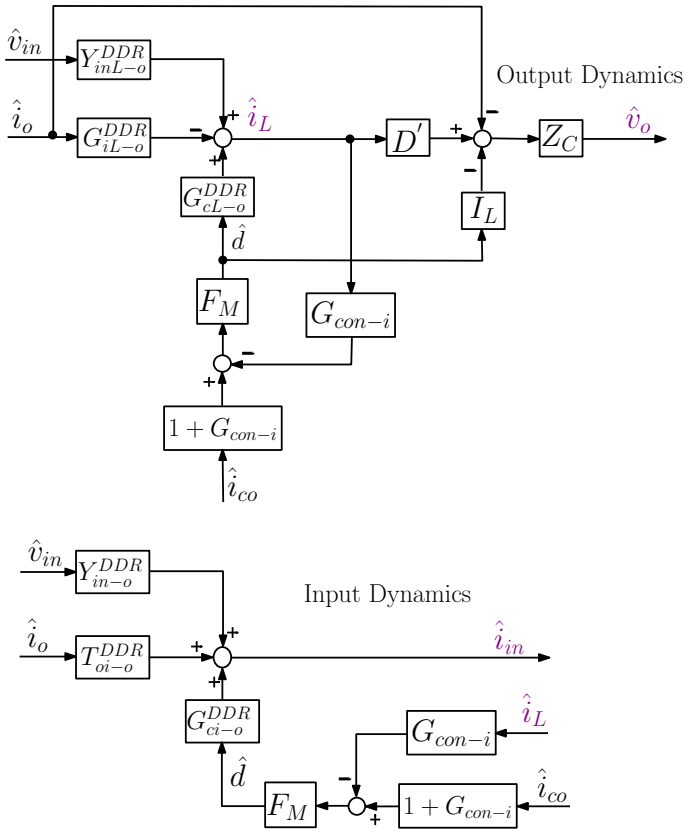


Figure 3.10. *Control block diagram for ACM-controlled boost converter*

where Z_c is the output capacitor impedance, $D^{'}$ and I_L are the steady-state operating points solved in Chapter 2, $\hat{i}_{co}$ is the output of the outer controller in the current-domain. Y_{inL-o}^{DDR}, G_{iL-o}^{DDR} and G_{cL-o}^{DDR} are the input-to-state transfer functions under DDR control which are computed in Equation 3.2.5.

3.3.4 Dynamic Models of ACM-Controlled Boost Converter at Open loop

The open loop dynamic transfer functions under ACM control can be computed predicated on the DDR dynamics by changing the duty ratio to the duty ratio constraints for ACM control (i.e., Equation 3.14) [29, p. 228], which yields:

$$\begin{aligned}\hat{i}_{in}^{ACM} &= Y_{in-o}^{ACM}\hat{v}_{in} + T_{oi-o}^{ACM}\hat{i}_o + G_{ci-o}^{ACM}\hat{c} \\ \hat{v}_o^{ACM} &= G_{io-o}^{ACM}\hat{v}_{in} - Z_{o-o}^{ACM}\hat{i}_o + G_{co-o}^{ACM}\hat{c}\end{aligned} \tag{3.15}$$

where

$$\begin{bmatrix} Y_{in-o}^{ACM} & T_{oi-o}^{ACM} & G_{ci-o}^{ACM} \\ G_{io-o}^{ACM} & -Z_{o-o}^{ACM} & G_{co-o}^{ACM} \end{bmatrix} =$$

$$\begin{bmatrix} Y_{in-o}^{DDR} - (\dfrac{Fm(\dfrac{G_{c-i}G_{io-o}^{DDR}}{D^{'}Z_C})G_{ci-o}^{DDR}}{1+L_c}) & T_{oi-o}^{DDR} + (\dfrac{Fm(\dfrac{G_{c-i}Z_{o-o}^{DDR}}{D^{'}Z_C} - \dfrac{G_{c-i}}{D^{'}})G_{ci-o}^{DDR}}{1+L_c}) & \dfrac{(1+G_{c-i})F_mG_{ci-o}^{DDR}}{1+L_c} \\ \dfrac{(1+\dfrac{I_LF_mG_{c-i}}{D^{'}})G_{io-o}^{DDR}}{1+L_c} & \dfrac{(1+\dfrac{I_LF_mG_{c-i}}{D^{'}})Z_{o-o}^{DDR} + \dfrac{F_mG_{c-i}}{D^{'}}G_{co-o}^{DDR}}{1+L_c} & \dfrac{(1+G_{c-i})F_mG_{co-o}^{DDR}}{1+L_c} \end{bmatrix}$$

where $L_c = G_{c-i} F_m G_{cL-o}^{DDR}$ represents the inductor current loop gain [29, p. 230].

The corresponding set of special transfer functions for ACM (3.16) can be drawn based on the generalized form in Equation 2.19, where the original open loop transfer functions are replaced with the ACM transfer functions.

$$\begin{bmatrix} Y_{in-sco}^{ACM} & Y_{in-\infty}^{ACM} & T_{oi-\infty}^{ACM} \\ Z_{o-oci}^{ACM} & -Z_{o-\infty}^{ACM} & G_{io-\infty}^{ACM} \end{bmatrix} = \begin{bmatrix} Y_{in-o}^{ACM} + \frac{G_{io-o}^{ACM} T_{oi-o}^{ACM}}{Z_{o-o}^{ACM}} & Y_{in-o}^{ACM} - \frac{G_{io-o}^{ACM} G_{ci-o}^{ACM}}{G_{co-o}^{ACM}} & T_{oi-o}^{ACM} + \frac{Z_{o-o}^{ACM} G_{ci-o}^{ACM}}{G_{co-o}^{ACM}} \\ Z_{o-o}^{ACM} + \frac{G_{io-o}^{ACM} T_{oi-o}^{ACM}}{Y_{in-o}^{ACM}} & Z_{o-o}^{ACM} + \frac{T_{oi-o}^{ACM} G_{co-o}^{ACM}}{G_{ci-o}^{ACM}} & G_{io-o}^{ACM} - \frac{Y_{in-o}^{ACM} G_{co-o}^{ACM}}{G_{ci-o}^{ACM}} \end{bmatrix} \tag{3.16}$$

According to the output dynamics expressed in Equation 3.15, the roots location of the common denominator $(1 + L_c)$, also known as the characteristic polynomial of the system, determines the system stability, because the position of the roots in the complex-plane describes how the exponential function behaves in time-domain [6]. Recall the theory background introduced in Chapter 2, the system is stable if the roots located in the LHP (i.e., poles of the system are complex values that contain negative real parts) while it becomes unstable when the roots positioned in the RHP (i.e., the system includes poles with positive real parts). When the roots located in the imaginary axis, the system is marginal stability in control engineering, which means that the time-domain transient will oscillate with a constant amplitude.

3.3.5 Input Impedance Transfer Function of ACM-Controlled Boost Converter at Closed-Loop

The input impedance transfer function of the ACM-controlled DC-DC boost converter at closed loop is acquired on the basis of the input impedance at open loop (Y_{in-o}^{ACM}), which is expressed below:

$$Y_{in-c}^{ACM} = \frac{Y_{in-o}^{ACM}}{1 + L_v} + \frac{L_v}{1 + L_v} Y_{in-\infty}^{ACM} \tag{3.17}$$

where the voltage control loop gain is $L_v = G_{co-o}^{ACM} G_{c-v} H_v G_s$. $G_s = \dfrac{1}{R_s}$ denotes the modulator gain, and the ideal input impedance is:

$$Y_{in-\infty}^{ACM} = Y_{in-o}^{ACM} - \frac{G_{io-o}^{ACM} G_{ci-o}^{ACM}}{G_{co-o}^{ACM}}$$

The open loop input-to-output noise attenuation could be very high under different CMC (i.e.,$G_{io-o}^{ACM} \approx 0$), which indicates that the converter dynamics is invariable with respect to the source disturbance [11]. As a result, $Y_{in-c}^{ACM} \approx Y_{in-o}^{ACM} \approx Y_{in-\infty}^{ACM}$ when $G_{io-o}^{ACM} \approx 0$ [29, p. 240]. Thus, Y_{in-o}^{ACM} is dominating in the input impedance under ACM control at closed loop.

4 CONTROL DESIGN IN SIMULINK ENVIRONMENT

This chapter introduces the control design principles briefly. Based on these principles, proper compensators can be designed for the DDR and ACM-controlled boost converter operating in CCM with Matlab.

4.1 Control Design Principles

Proportional-integral-derivative (PID) controller as well as proportional-integral (PI) controller are widely utilized for feedback control in general. PID controller is required in DDR because of the resonant nature of the open loop DC-DC boost converter operates in CCM (i.e., an RHP-zero is included in the control-to-output transfer function) [28] while PI controller is adequate to use in CMC, as CMC is a dual-loop control that enables both voltage and current outputs control [21]. This section introduces how the PID controller works and how to design the controller transfer function with loop shaping techniques.

4.1.1 Working Principle of PID Controller

Figure 4.1 illustrates the framework of a PID controller that comprised of proportional, integral, and derivative parts. It brings the output variable to a target level by correcting the difference between the desired value and a sensed value, which is the error value.

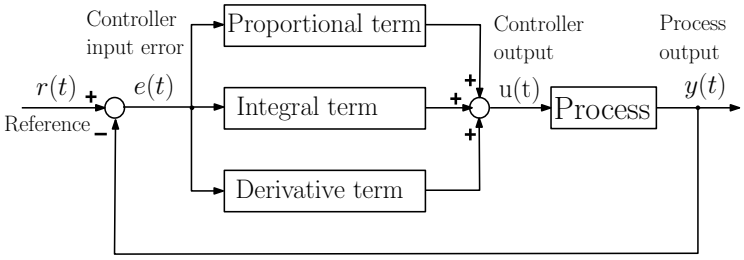


Figure 4.1. *Basic structure of PID controller*

The expressions of PID controller in frequency-domain and in time-domain are described in Equation 4.6. The proportional term is responsible for amplifying the current error value while an integral term is essential to eliminate steady-state error resulting from the pure proportional part, and the derivative term is able to enhance the system transient performance [10].

PID controller expression in time-domain:

$$G_{PID}(t) = K_p e(t) + K_i \int_0^t e(\tau)d\tau + K_d \frac{de(t)}{dt} \tag{4.1}$$

PID controller expression in frequency-domain:

$$G_{PID}(s) = K_p + \frac{K_i}{s} + K_d s$$

where K_p, K_i, and K_d denote the proportional gain, the integral gain and the derivative gain, respectively. The error signal $e(t)$ comes from the difference between the setpoint and the process

variable. t is the time while τ is the variable of integration. In the expression of frequency-domain, s denotes the complex frequency.

Proportional-integral (PI) controller is actually a kind of PID controller without a derivative term. It is fairly useable in ACM control due to the high sensitivity of the derivative item to the measurement noise whereas the system may fail in reaching its target value if the integral term is lost.

4.1.2 Loop Shaping Principles

The idea of loop shaping is used to design the controllers in the frequency-domain since the controller poles and zeros influence the shape of the control loop gain which reflects the system stability. The loop shaping is done by adjusting the parameters of the compensator to reach the desired loop gain shape. For example, zeros are used to boost phase margin while poles can reduce gain margin, and controller gain (K) is used to set crossover frequency. PI compensator is applied as the feedback mechanism in ACM control and is represented as Equation (4.2). It is notable that the transfer function of the used PI controller is required to have at least as many poles as it has zeros to be realizable. [5]

$$G_{PI}(s) = \frac{K(\frac{s}{\omega_{zero}} + 1)}{s(\frac{s}{\omega_{pole}} + 1)} \tag{4.2}$$

In general, loop shaping can be done by following the steps below:

1. Plot the uncompensated control loop gain (i.e., $G_{PI}(s) = 1$).
2. Specify the desired crossover frequency and expected phase margin. Normally, $45°$ to $60°$ is enough to ensure a stable operation.
3. Boost the phase of the loop gain by placing Left-hand Plane (LHP) zeros and LHP-poles.
4. Adjust the gain (K) to a value that gives the desired crossover frequency to the loop gain. This gain value can be calculated from $K = 10^{\frac{\pm dB}{20}}$, where $\pm dB$ is the required magnitude we intend to boost or decrease with respect to the uncompensated loop gain magnitude.

As long as the proper zeros, poles and gain value are settled, the control loop is supposed to stabilize the transient response of the converter, which can be verified by the simulation results.

4.2 Switching Model of Open Loop Switched-mode Boost Converter

In the light of the dynamic models constructed in Chapter 2, the corresponding model shows the power stage of the switched-mode boost converter is built in Simulink, and the characteristics of the system would be demonstrated by various plots, for example, the frequency response can be displayed by bode plots.

4.2.1 Building Switching Model of the Power Stage of Boost Converter

The switching model of the boost power stage is built founded on the steady-state averaged model introduced in Chapter 2. The instantaneous state variables are obtained for on-time and off-time separately. The converter operates in CCM if there is no limitation for the state variable values. [29, p. 279]

Equation 4.3 presented the derivatives of the state variables and the relations between output variables and circuit variables.

$$\begin{aligned}&\text{During On-time:}\\ \frac{di_L}{dt} &= \frac{1}{L}(V_{in} - r_L i_L - r_{ds} i_L)\\ \frac{dv_C}{dt} &= \frac{1}{C}(V_o - r_C i_C)\\ i_{in} &= i_L\\ v_o &= v_C - r_C i_o\end{aligned} \tag{4.3}$$

$$\begin{aligned}&\text{During Off-time:}\\ \frac{di_L}{dt} &= \frac{1}{L}(V_{in} - r_L i_L - R_d i_L - V_D - r_C i_C - V_c)\\ \frac{dv_C}{dt} &= \frac{1}{C}(V_o - r_C i_C)\\ i_{in} &= i_L\\ v_o &= v_C + r_C i_L - r_C i_o\end{aligned}$$

The power stage of the switched-mode boost converter in Simulink is displayed in Appendix A. The selector switch works in the way that it will pass through the top input (T) when the control input port satisfies the selected criterion, otherwise, it will pass through the bottom input (F). In this simulation, the duty ratio (d) is 1 for on-time and 0 for off-time. Thus, 0.5 can be set as the threshold for the selector switches to distinguish on and off-time operation. The saturation levels are not defined in the integrator because the converter only operates in CCM. [29]

4.2.2 Component Sizing of the Boost Converter

Component sizing is a significant part of the converter building. There are principles that need to be followed in this part. For example, the inductor and capacitor are sized according to the requirement on the maximum allowed peak-to-peak inductor current ripple and the maximum output voltage ripple, respectively. For the purpose of determining the proper value for the memory elements, basic circuit parameters utilized in the Simulink model are first defined in Table 4.1.

Table 4.1. *Basic Circuit Parameters used for Simulation.*

Basic Circuit Parameter	Value
DC Input voltage (V_{in})	$20V$
Output current (I_o)	$1.5A$
Output voltage reference (V_{o-ref})	$75V$
Switching frequency (f_s)	$100kHz$

Inductor is utilized to preserve constant current in the switched-mode boost converter while the capacitor is added to minimize the output voltage ripple as well as maintain a constant voltage level. The power losses in the inductor and capacitor are mainly as a result of the equivalent series resistance (ESR), therefore, lower ESR is preferred to have lower power losses. [1]

The value of the minimum inductance can be approximately solved as:

$$L_{min} = \frac{V_{in} T_s D}{I_{L-pp}} \tag{4.4}$$

where I_{L-pp} is the maximum allowed peak-to-peak inductor current ripple, and D denotes the steady-state duty ratio. Generally, the limitation for the ripple of inductor current is estimated in the range of 20% to 40% . The corresponding inductor current ripple is computed as $I_{L-pp} = 30\% \frac{V_o I_o}{V_{in}}$ and the minimum inductance value calculated is $89.414\mu H$. As a result,

$350\mu H$ (approximately four times of the minimum value) is a good option in the present case for the inductance value.

Similarly, the value for the output capacitor can be solved as:

$$C_{min} = \frac{I_o T_s D}{V_{C-ripple}} \tag{4.5}$$

Where $V_{C-ripple}$ is the maximum output voltage ripple. According to the related standard IEEE 519, the ripple of output voltage should be limited in the range of 2%. The corresponding capacitance value calculated is $7.5443\mu F$. However, with this minimum capacitance value, the resonant frequency of G_{co-o} is $756kHz$ at input voltage of $20V$ as displayed in Figure 4.2, this will lead to unstable operation of the system if the controller is too fast and the system reacts during the opposite direction period.

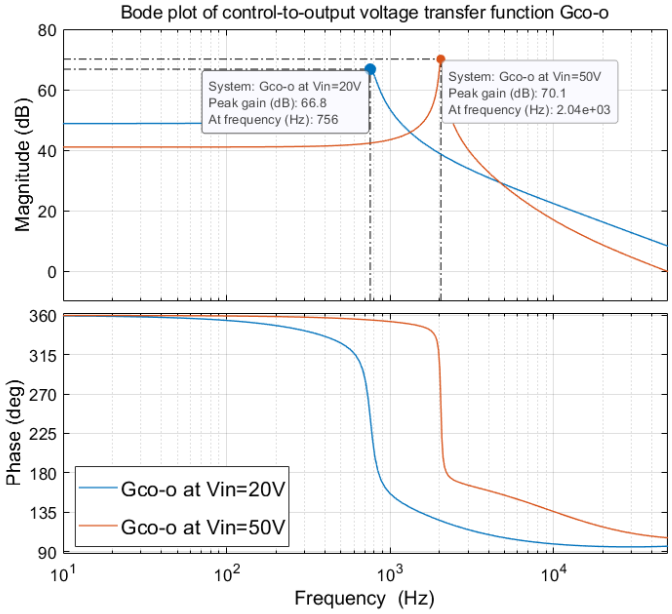


Figure 4.2. *Bode diagram of control-to-output transfer function at open loop with minimum capacitance*

As the output capacitance increases, the resonant frequency decreases. Thus, a higher capacitor value $(316\mu F)$ is applied to guarantee stable operation. Figure 4.3 illustrated the lower resonant frequency $(86.1Hz)$ of G_{co-o} with modified capacitance. As the resonant frequency is significantly decreased, the boost converter is capable to operate stably.

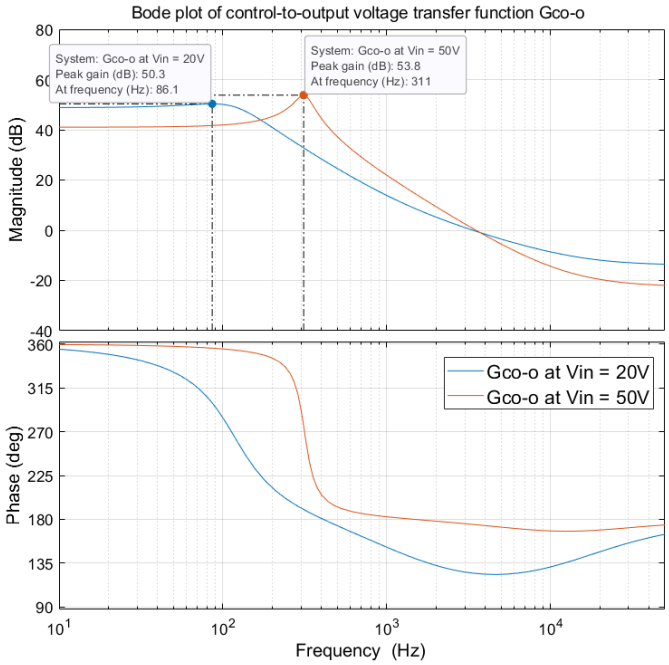


Figure 4.3. *Bode diagram of control-to-output transfer function at open loop with modified capacitance*

Power losses in a power diode are consist of conduction power loss as a consequence of the forward voltage drop, switching power loss led by the switching actions of the diode, and reverse leakage current power loss occurs when the diode is reversed biased [1]. The parameters for the diode and the switching transistor can be chosen based on the datasheet of the components applied for different applications. The passive components parameters utilized in the Simulink model are epitomized in Table 4.2.

Table 4.2. *Passive Components Parameters used for Simulation.*

Circuit Parameter	Value
Inductor vlaue (*L*)	$350\mu H$
Inductor resistance (r_L)	$1m\Omega$
Capacitor value (*C*)	$316\mu F$
Capacitor resistance (r_C)	$33m\Omega$
Forward voltage drop on diode (V_D)	$0.3V$
Diode resistance (R_d)	$55m\Omega$
Transistor switching resistance (r_{ds})	0.3Ω

4.2.3 Frequency Response of Transfer Functions at Open Loop

Figure 4.4 depicts the existence of an RHP-zero in G_{co-o}, which would limit the control-bandwidth of the feedback control loop gain as a consequence of the phase behavior of G_{co-o} in high-frequency region [29, p. 325].

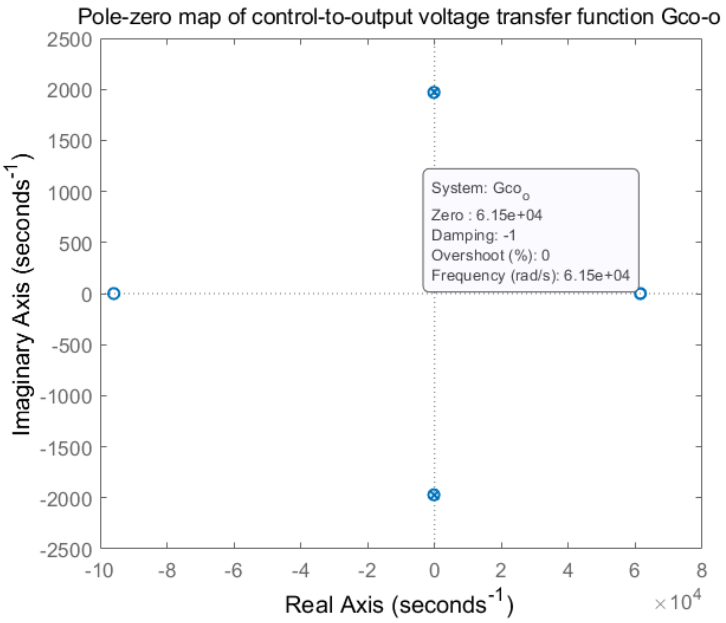


Figure 4.4. *Pole-zero map of open loop control-to-output transfer function with modified capacitance*

The corresponding open loop output impedance at varying voltage is displayed in Figure 4.5. The difference of the output impedance curve forecasts that the transient performance in time-domain at varying input voltage will be different.

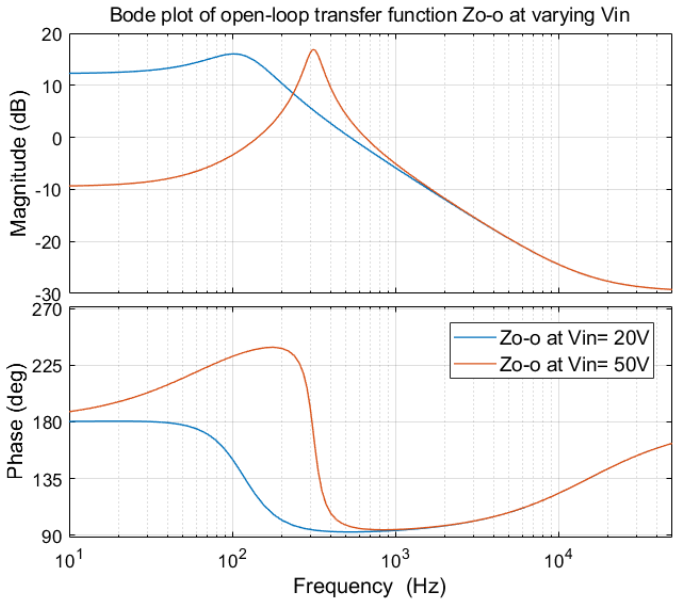


Figure 4.5. *Bode plot of open loop output impedance transfer function at varying voltage*

4.3 Control Design in Simulink Environment

Targeting on the power stage of the switched-mode boost converter built in the last section, the corresponding compensators for DDR control and for ACM control are designed in this part. The objective of this section is to verify if the transient response corresponds to the prediction of the frequency response, which further validates the correctness of the dynamic models derived in

4.3.1 Principles for Designing the Control-Loop Crossover Frequency

The system step response goes first in the "wrong" direction when there is an RHP-zero in the open loop G_{co-o}. Thus, when designing the controller of this system, the bandwidth of the control loop is necessary to be lower than the RHP-zero frequency ($1.4889kHz$) to guarantee stable operation [29, p. 325].

PID and PI controllers are most often applied in designing the feedback control of voltage-fed converters. PI controller is allowed to use when there is no resonant behavior in the converter, it is capable to boost adequate phase for achieving the desired phase margin [29, p. 278]. The principles that usually need to be followed for designing the feedback-loop crossover frequency are listed below [29, p. 322]:

1. The crossover frequency is ought to be at least three times the imaginary resonant frequency ($3f_{res}$) of the converter for avoiding ringing behaviors (i.e., oscillation of a signal) caused by the resonance, where the imaginary resonant frequency is solved as

$$f_{res} = \frac{\omega_{res}}{2\pi} \text{ where } \omega_{res} = \frac{D^{'}}{\sqrt{LC}}$$

2. The crossover frequency is supposed to be lower than at least one-fifth of f_s in order to prevent the switching ripple which may result in instability by affecting the duty ratio generation.

3. The crossover frequency cannot be more than the RHP zero frequency of G_{co-o} in the case of RHP-zero exists in the dynamics of the converter.

$$f_{co-max} = f_{RHP-zero} = \frac{\omega_{RHP-zero}}{2\pi} \text{ where } \omega_{RHP-zero} \approx \frac{V_{in}}{LI_L}$$

4. In the case of RHP-pole exists in the dynamics of the converter, the crossover frequency cannot be less than the frequency of RHP-pole.

4.3.2 Control Design for DDR-controlled Boost Converter

The steady-state operating points, related transfer functions and the control circuit schematics for designing the DDR controller are presented in Chapter 4. As given in Figure 4.4, there is an RHP-zero in G_{co-o}, which would limit the crossover frequency of the voltage control loop to a lower value [29, p. 321]. In addition, a PID converter is required in this case as a consequence of the resonant nature of the boost converter [28], whose transfer function can be expressed as:

$$G_{PID}(s) = \frac{K(\frac{s}{\omega_{zero-1}} + 1)(\frac{s}{\omega_{zero-2}} + 1)}{s(\frac{s}{\omega_{pole-1}} + 1)(\frac{s}{\omega_{pole-2}} + 1)} \tag{4.6}$$

Simulink model of DDR-controlled boost converter in Appendix A displays the connections between the DDR voltage controller and the boost converter, where the power stage model is shown as a subsystem. The implementation of the DDR voltage compensator with PWM modulator is also shown in Appendix A. A repeating sequence is employed to produce the PWM ramp signal, where the cycle time ($T_s = \frac{1}{f_s}$) and the magnitude ($V_M = 3$) of the ramp are specified. Output voltage sensing gain (H_v) is assumed to be unity. The compensators are implemented by using the transfer function of a PID controller, where the control parameters (gain values, zeros and poles) are specified later.

The output voltage feedback loop gain can be computed as:

$$\begin{aligned} L_v^{DDR} &= H_v G_{PWM} G_{con} G_{co-o}^{DDR} \\ &= H_v \frac{1}{V_M} \frac{K_v(\frac{s}{\omega_{z1}}+1)(\frac{s}{\omega_{z2}}+1)}{s(\frac{s}{\omega_{p1}}+1)(\frac{s}{\omega_{p2}}+1)} \frac{\frac{I_o}{D'LC}(\frac{D^{'2}V_1}{I_o} - r_1 - sL)(1+sr_C C)}{s^2 + s\frac{r_1}{L} + \frac{D^{'2}}{LC}} \end{aligned} \tag{4.7}$$

The aim of the DDR control design is to have as high as possible crossover frequency that is lower than the RHP-zero frequency and to yield a proper phase margin (i.e., $PM > 40^\circ$) as well as gain margin (i.e., $GM > 6dB$). According to the limitations for the control design presented in Section 4.3.1, the expected crossover frequency for the outer control loop is set in the range of $353Hz$ to $14.889kHz$. To achieve this goal, the controller zeros (ω_{z1}, ω_{z2}) are placed before the imaginary resonant frequency at ($0.5\omega_{res}$), then the first control pole (ω_{p1}) is placed at the frequency of the zero ($\omega_{ESR-zero} = \frac{1}{r_C C}$) which is resulting from the capacitor (C) and its Equivalent series resistance (ESR), i.e., $\omega_{p1} = 30\omega_z$. The second pole is placed at $\omega_{p2} = \frac{\omega_s}{8}$. The control parameters used for the simulation of closed loop DDR control are epitomized in Table 4.3.

Table 4.3. *Voltage Feedback Control Parameters used for DDR Closed-loop Simulation.*

DDR voltage control parameters	
Control Gain (K_v)	8
First Zero (ω_{z1})	$358Hz$
Second Zero (ω_{z2})	$358Hz$
First Pole (ω_{p1})	$10.74kHz$
Second Pole (ω_{p2})	$78.54kHz$

The bode plot of the shaped DDR voltage control loop gain when the input voltage equals to $20V$ and $50V$ is illustrated in Figure 4.6. With the adjusted parameters for the controller, the loop gain transfer function is shaped to an expected performance achieving the gain margin of $7.73dB$, phase margin of 49°, and crossover frequency of $537Hz$ at $V_{in} = 20V$. Actually, the crossover frequency is limited by the magnitude behavior at the high-frequency region of the control loop gain to roughly half the RHP-zero frequency [29, p. 326]. In addition, it is evident that the input voltage has a considerable impact on the crossover frequency as well as the resonance, i.e., the crossover frequency and the resonance both increase with the increasing input voltage.

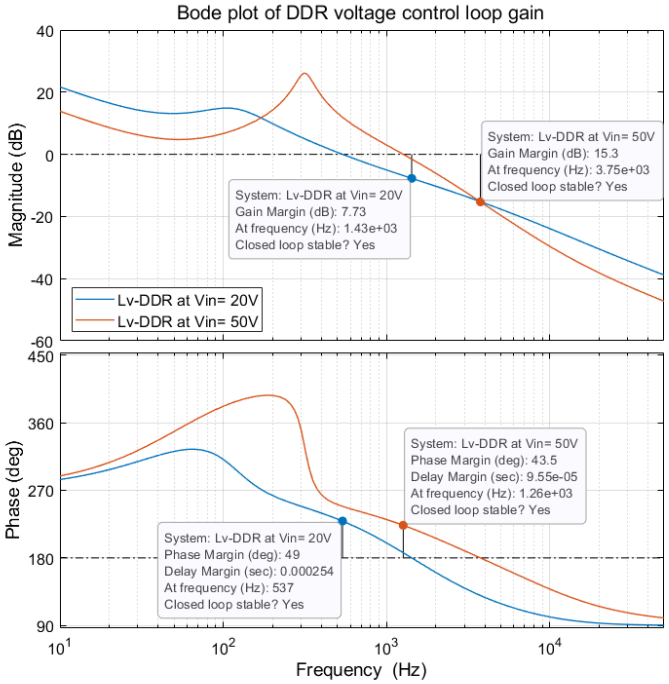


Figure 4.6. *Bode plot of shaped DDR voltage control loop gain at varying input voltage*

Figure 4.7 illustrates the output impedance behavior under DDR control at closed loop, its corresponding output impedance value is 0.739Ω at $V_{in} = 20V$ and 0.2359Ω at $V_{in} = 50V$, respectively. This impedance value implies that a voltage dip will be induced in the load transient response as the load current increases.

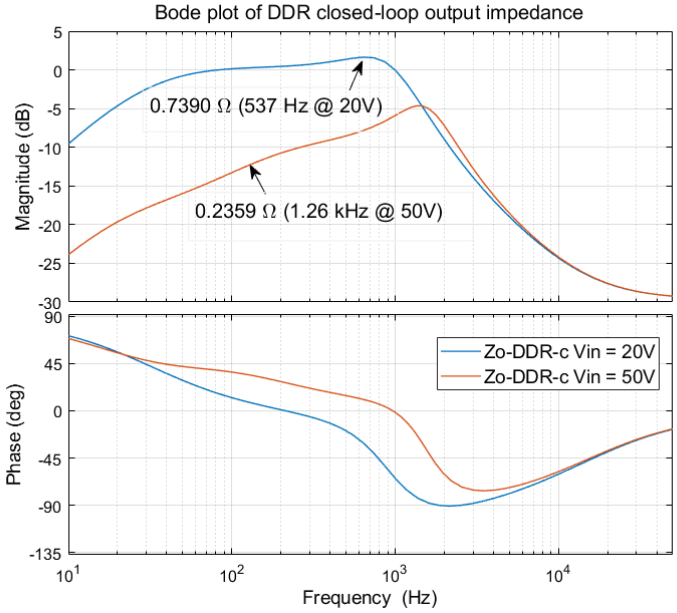


Figure 4.7. *Bode plot of DDR closed loop output impedance at varying input voltage*

When a step change occurs in the load current from $0.75A$ to $1.5A$, the corresponding output voltage step response at input voltage of $20V$ and $50V$ is displayed in Figure 4.8. The predicted voltage dip at $V_{in} = 20V$ can be calculated as $V_{dip} = 0.5542V$ according to the output impedance

value (0.739Ω) at closed loop and the output current change while the corresponding voltage dip in the simulation result is $0.78V$. Similarly, the predicted voltage dip at $V_{in} = 50V$ is $0.1769V$ with the closed loop output impedance value equals to 0.2359Ω, the corresponding voltage dip in the simulation result is $0.38V$. The slight difference ($0.2258V$ at $V_{in} = 20V$ and $0.2031V$ at $V_{in} = 50V$) between the predicted value and the simulation shows that predictions based on the small-signal models are roughly correct but not precise enough. In addition, the RHP-zero in the output dynamics of the switched-mode boost converter makes it impossible for the frequency response to accomplish fast setting transient and small voltage dips simultaneously [29, p. 324].

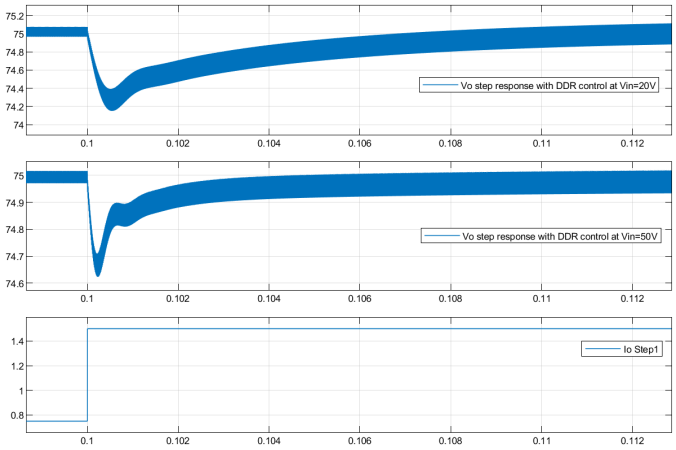


Figure 4.8. *Output voltage step response of DDR-controlled boost converter at varying* V_{in}

4.3.3 Control Design for ACM-controlled Boost Converter

The first objective of designing a proper ACM controller is to design an inner loop compensator G_{c-i}. The design process starts by finding out the converter transfer function within the inductor current and the duty cycle. Through the open loop transfer function matrix studied in Chapter 2, we can understand how $\hat{d}$ perturbation affects the output variable, i.e., inductor current, where $\hat{d}$ represents a small-signal perturbation that injected into the duty cycle. Then the inductor current control loop can be stabilized by applying the loop shaping techniques to the inner compensator. Once the inductor current controller is tuned properly (i.e., the frequency response of inductor control loop gain L_c obtained the desired crossover frequency as well as acceptable stable margins), the output voltage loop is required not only to stabilize the operation of the inner current loop control, but also provide the reference to the inductor current. The outer voltage loop compensator is tuned similarly as the current loop compensator until an expected frequency response of voltage control loop gain (L_v) is obtained.

The connections between the ACM current as well as voltage controllers and the boost converter in Simulink are given in Appendix A, where the power stage model is shown as a subsystem. The implementation of the inner current compensator with PWM modulator and outer voltage compensator is also shown in Appendix A. A repeating sequence is utilized to generate the PWM ramp signal, where the cycle time ($T_s = \frac{1}{f_s}$) and the magnitude ($V_M = 3$) of the ramp are specified. R_s (0.15Ω) is the sensing resistor for the inductor current. The compensators are implemented by using the transfer function of a PI controller, where the control parameters (i.e., zeros, poles and gain values) are specified later.

The inductor current feedback loop gain can be computed as:

$$\begin{aligned} L_c^{ACM} &= G_{PWM} G_{c-i} G_{cL-o}^{DDR} \\ &= \frac{1}{V_M} \frac{K_i(\frac{s}{\omega_{zi}} + 1)}{s(\frac{s}{\omega_{pi}} + 1)} \frac{I_o + CV_1 s}{(D'^2 + CLs^2 + Cr_1 s)} \end{aligned} \tag{4.8}$$

where $V_1 = V_o + V_D + (R_d - r_{ds} + Dr_C)\frac{I_o}{D'}$. G_{PWM} is the PWM gain. G_{cL-o}^{DDR} is the control-to-state transfer function under DDR control. G_{c-i} denotes the transfer function of the inductor current controller.

The output voltage feedback loop gain can be computed as:

$$\begin{aligned} L_v^{ACM} &= H_v G_a G_{c-v} G_{co-o}^{ACM} \\ &= H_v \frac{1}{R_s} \frac{K_v(\frac{s}{\omega_{zv}} + 1)}{s(\frac{s}{\omega_{pv}} + 1)} \frac{(1 + G_{c-i}) F_m G_{co-o}^{DDR}}{1 + L_c^{ACM}} \end{aligned} \tag{4.9}$$

where the modulator gain G_a is usually equated to $\frac{1}{R_s}$. H_v denotes the sensing gain of output voltage. G_{c-v} is the output voltage controller transfer function. G_{co-o}^{ACM} is the control-to-output transfer function under ACM control.

The desired crossover frequency of the inductor current control loop is normally placed around one-tenth of the switching frequency (i.e., $f_{coi} < 10kHz$). The output voltage control is supposed to be slower than the current control so that the inductor current is able to follow its reference before the control signal changes. With regard to the output voltage control loop, the maximum crossover frequency (f_{cov}) is also limited to the RHP-zero frequency of the switched-mode boost converter ($f_{RHP-zero}$). Thus, the desired crossover frequency (f_{cov}) for the voltage control loop is set below $1.4889kHz$. Furthermore, a good design is expected to yields an adequate phase margin and at least $6dB$ of the gain margin.

Based on these design limitations, the zero of the voltage controller (ω_{zv}) is set at half of the imaginary resonant frequency (i.e., $\omega_{zv} = 0.5\frac{D^{'}}{\sqrt{LC}}$). The controller pole locates at $\frac{\omega_s}{8}$ to achieve acceptable PM. The control parameters used for the simulation of closed loop ACM control are epitomized in Table 4.4.

Table 4.4. *ACM Control Parameters used for Simulation.*

Current control parameter		Voltage control parameter	
Zero (ω_{zi})	$738.6Hz$	Zero (ω_{zv})	$369.2Hz$
Pole (ω_{pi})	$29.54kHz$	Pole (ω_{pv})	$12.5kHz$
Control Gain (K_i)	388	Control Gain (K_v)	100

The shaped inductor current control loop gain (L_c) at varying input voltage is displayed in Figure 4.9, while shaped output voltage control loop gain (L_v) is shown in 4.10. The obtained crossover frequency ($f_{cov} = 635Hz$) of the voltage feedback loop gain at $V_{in} = 20V$ is below half ($744.458Hz$) of the frequency of RHP-zero ($1.4889kHz$), which is limited by the magnitude behavior of the control loop gain at high-frequency region [29, p. 326]. On the other hand, the obtained f_{cov} is a bit higher than the voltage control loop crossover frequency ($537Hz$) of the boost converter under DDR-control. Since the GM more than $6dB$ and the PM more than $40°$ are required for stable operation, the obtained GM and PM meet the expectations perfectly.

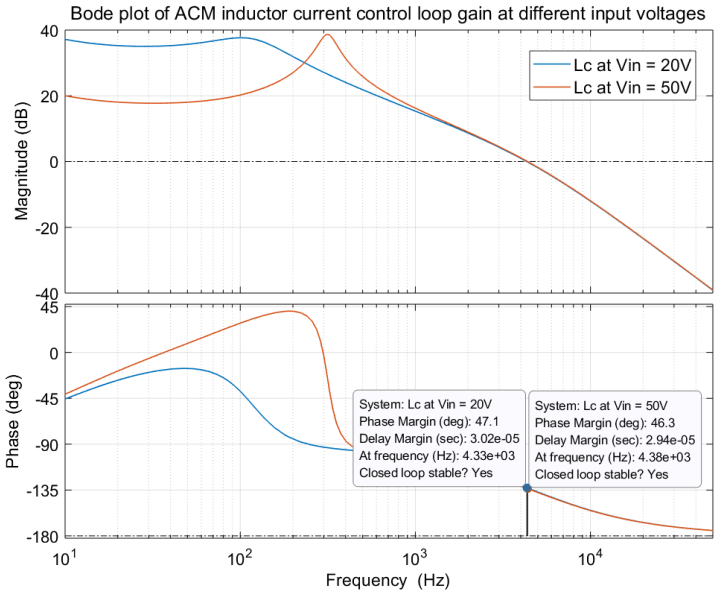


Figure 4.9. *Bode plot of shaped ACM inductor current control loop gain*

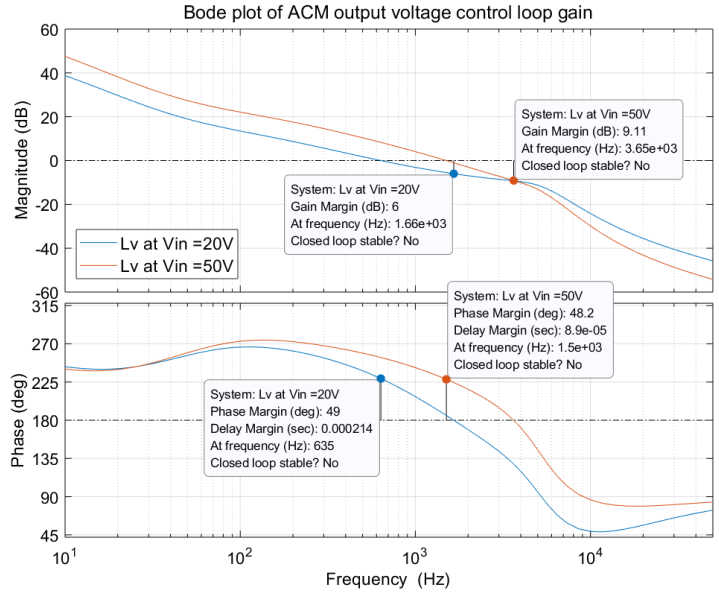


Figure 4.10. *Bode diagram of shaped ACM output voltage control loop gain*

Figure 4.11 illustrates the output impedance behavior under ACM control at closed loop. At input voltage of $20V$ and crossover frequency of $635Hz$, the output impedance value at closed loop is 0.5161Ω. Accordingly, the predicted voltage dip can be computed as $V_{dip} = 0.3871V$ while the corresponding voltage dip in the simulation result is $1V$. Similarly, the closed loop output impedance at $V_{in} = 50V$ is 0.2553Ω which yields a predicted voltage dip equals $0.1915V$, and the simulated voltage dip is $0.5V$. There is a slight difference ($0.6129V$ at $V_{in} = 20V$ and $0.3085V$ at $V_{in} = 50V$) between the prediction and simulation, which means that the small-signal dynamic model is basically correct but lacks accuracy.

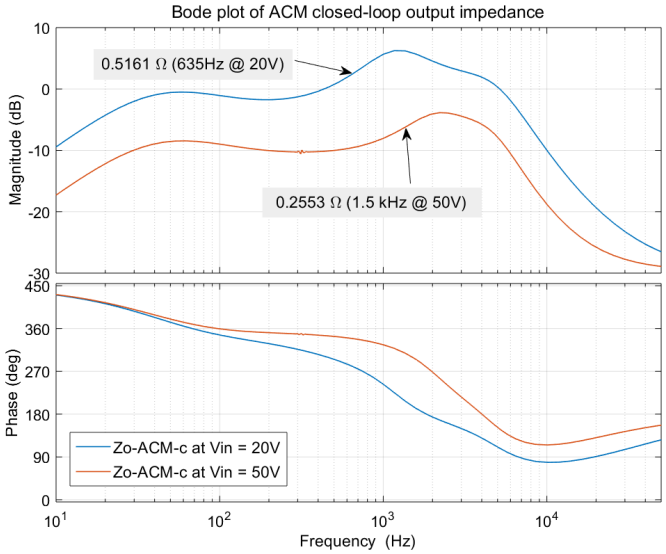


Figure 4.11. *Bode diagram of closed loop output impedance under ACM control at varying input voltage*

The output voltage step responses with the ACM controller when the load current changes from half to full value is illustrated in Figure 4.12. The initial dip in the transient performance of the output voltage is related to the magnitude of the closed-loop output impedance value at frequency f_{cov}. Compared to the transient performance under DDR control, the step response under ACM control contains more oscillations since the inductor current feedback loop is more sensitive to the input changes.

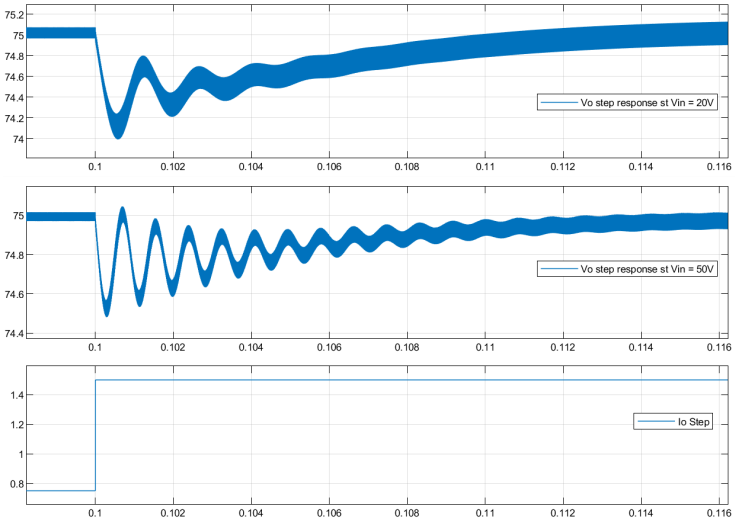


Figure 4.12. *Output voltage step response of the boost converter with the ACM controller at varying input voltage*

This chapter presented the DDR and ACM control design for boost converter in the Simulink environment specifically. The obtained control loop gain satisfied expectations for stable operation. The correctness of the dynamic models derived in Chapter 3 are demonstrated by the simulation results, founded on the fact of the correspondence between the frequency response and output voltage step response. However, the slight difference ($0.6129V$ at $V_{in} = 20V$ and $0.3085V$ at $V_{in} = 50V$) between the predicted voltage dip and the simulated dip value shows that the small-signal dynamic models are not perfectly accurate.

5 DYNAMIC MODELING OF FILTER-CONVERTER INTERCONNECTED SYSTEM

An excellent control design improves the performance of the converter significantly. However, it does not always result in robust stability and outstanding transient response due to the influence of the external interactions, such as input electromagnetic interference (EMI) filter [26, p. 302].

The connection of an input filter allows reducing the switching noises and prevent EMI from disturbing the controller performance. However, the input EMI filter and the switched-mode converters form an interconnected system, and the interactions between them may lead to instability and unwanted dynamic performance without proper design [13]. The key to analyzing the stability of the cascaded system, i.e., impedance ratio (also named minor loop gain), is computed in this chapter.

5.1 Filter-Converter Interconnected Systems

This section introduces the dynamic models of the filter-converter cascaded system as well as computes the minor-loop gain.

5.1.1 Resonant LC-type Circuit as the Input Filter

Electromagnetic interference (EMI) is an inherent nature of the switched-mode converters due to the switching actions of the transistors [29, p. 225]. Hence, an input EMI filter is usually equipped for the converters to reduce the EMI noise in order to conform to the relevant EMI standards. LC-type input filters are commonly applied in DC-DC converters to smooth the input currents to a proper level prescribed by the relevant EMI standards [29, p. 111]. Figure 5.1 illustrates the typical single-section LC-type resonant circuit topology used in voltage-fed applications, it is normally added to the input terminal of the switched-mode converters.

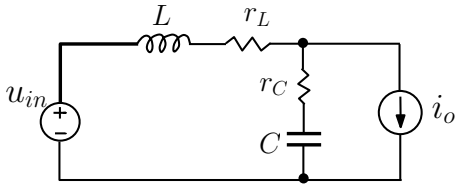


Figure 5.1. *Circuit topology of single-section LC-type resonant for voltage-fed applications*

The time-domain state space of the LC-type resonant circuit can be constructed as below, by following the State-Space Averaging (SSA) method introduced in Chapter 2.

$$\begin{aligned}
\frac{d\hat{i}_L}{dt} &= -\frac{r_L + r_C}{L}\hat{i}_L - \frac{1}{L}\hat{v}_C + \frac{1}{L}\hat{v}_{in} + \frac{r_C}{L}\hat{i}_o \\
\frac{d\hat{v}_C}{dt} &= \frac{1}{C}(\hat{i}_L - \hat{i}_o) \\
\hat{i}_{in} &= \hat{i}_L \\
\hat{v}_o &= \hat{v}_C + r_C\hat{i}_L - r_C\hat{i}_o
\end{aligned} \tag{5.1}$$

which can also be displayed in matrix form:

$$\begin{aligned}
\begin{bmatrix} \frac{d\hat{i}_L}{dt} \\ \\ \frac{d\hat{v}_C}{dt} \end{bmatrix} &= \underbrace{\begin{bmatrix} -\frac{r_L + r_C}{L} & -\frac{1}{L} \\ \frac{1}{C} & 0 \end{bmatrix}}_{\mathbf{A}} \begin{bmatrix} \hat{i}_L \\ \\ \hat{v}_C \end{bmatrix} + \underbrace{\begin{bmatrix} \frac{1}{L} & \frac{r_C}{L} \\ 0 & -\frac{1}{C} \end{bmatrix}}_{\mathbf{B}} \begin{bmatrix} \hat{v}_{in} \\ \\ \hat{i}_o \end{bmatrix} \\
\begin{bmatrix} \hat{i}_{in} \\ \\ \hat{v}_o \end{bmatrix} &= \underbrace{\begin{bmatrix} 1 & 0 \\ r_C & 1 \end{bmatrix}}_{\mathbf{C}} \begin{bmatrix} \hat{i}_L \\ \\ \hat{v}_C \end{bmatrix} + \underbrace{\begin{bmatrix} 0 & 0 \\ 0 & -r_C \end{bmatrix}}_{\mathbf{D}} \begin{bmatrix} \hat{v}_{in} \\ \\ \hat{i}_o \end{bmatrix}
\end{aligned} \tag{5.2}$$

Based on the time-domain state-space, the dynamic model of the voltage-fed LC-type input filter can be represented by [29, p. 111]:

$$\begin{aligned}
\begin{bmatrix} \hat{i}_{in} \\ \\ \hat{v}_o \end{bmatrix} &= \begin{bmatrix} Y_{inf} & T_{oif} \\ \\ G_{iof} & -Z_{of} \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \\ \\ \hat{i}_o \end{bmatrix} \\
&= \frac{\begin{bmatrix} sC & 1 + sr_C C \\ 1 + sr_C C & -(r_L + sL)(1 + sr_C C) \end{bmatrix}}{(s^2 LC + s(r_L + r_C)C + 1)} \begin{bmatrix} \hat{v}_{in} \\ \\ \hat{i}_o \end{bmatrix}
\end{aligned} \tag{5.3}$$

By comparing the common shared denominator of the input EMI filter transfer functions with the denominator of the second-order system, the resonant frequency (i.e., the frequency at where all the elements reach the peak value) of the input filter can be computed as:

$$\omega_{res} = \omega_n \sqrt{1 - 2\zeta^2} = \frac{1}{LC} \sqrt{1 - \frac{(r_L + r_C)^2 C}{2L}}$$

Founded on the dynamic transfer functions in Equation 5.8, the output impedance of the input EMI filter is obtained as:

$$Z_o^{LC} = \frac{\hat{v}_o}{\hat{i}_o} = \frac{(r_L + sL)(1 + sr_C C)}{(s^2 LC + s(r_L + r_C)C + 1)} \tag{5.4}$$

The set of input-to-state transfer functions of the LC-type input filter in matrix form is given by:

$$\begin{aligned}
\begin{bmatrix} \hat{i}_L \\ \\ \hat{v}_C \end{bmatrix} &= \begin{bmatrix} G_{iLf} & G_{oLf} \\ \\ G_{iCf} & -G_{oCf} \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \\ \\ \hat{i}_o \end{bmatrix} \\
&= \frac{\begin{bmatrix} \frac{s}{L} & \frac{1 + sr_C C}{LC} \\ \frac{1 + sr_C C}{LC} & -\frac{(r_L + sL)(1 + sr_C C)}{LC} \end{bmatrix}}{(s^2 + s\frac{(r_L + r_C)}{L} + \frac{1}{LC})} \begin{bmatrix} \hat{v}_{in} \\ \\ \hat{i}_o \end{bmatrix}
\end{aligned} \tag{5.5}$$

5.1.2 Dynamic Models of the Filter-affected Converter

Figure 5.2 displays the physical connection between the switched-mode boost converter and its input EMI filter, their dynamic models can be expressed as Equation 5.6 and Equation 5.7, respectively. The C_f and L_f represents the capacitor and inductor value of the LC-type input filter, while r_{Lf} and r_{Cf} are the ESR of the inductor and capacitor.

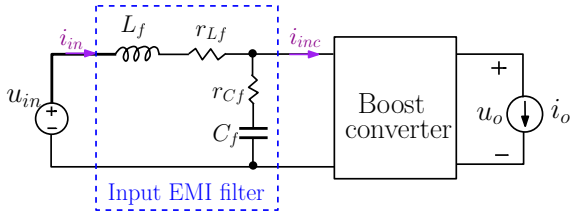


Figure 5.2. *Circuit topology of boost converter with an input EMI filter*

$$\begin{aligned}\hat{i}_x &= Y_{in-o}\hat{v}_x + T_{oi-o}\hat{i}_o + G_{ci-o}\hat{i}_{co} \\ \hat{v}_o &= G_{io-o}\hat{v}_x - Z_{o-o}\hat{i}_o + G_{co-o}\hat{i}_{co}\end{aligned} \tag{5.6}$$

$$\begin{aligned}\hat{i}_{in} &= Y_{in-f}\hat{v}_{in} + T_{oi-f}\hat{i}_x \\ \hat{v}_x &= G_{io-f}\hat{v}_{in} - Z_{o-f}\hat{i}_x\end{aligned} \tag{5.7}$$

The equivalent electrical two-port model is presented in Figure 5.3, which allows analyzing the impact of the input EMI filter on the boost converter dynamics.

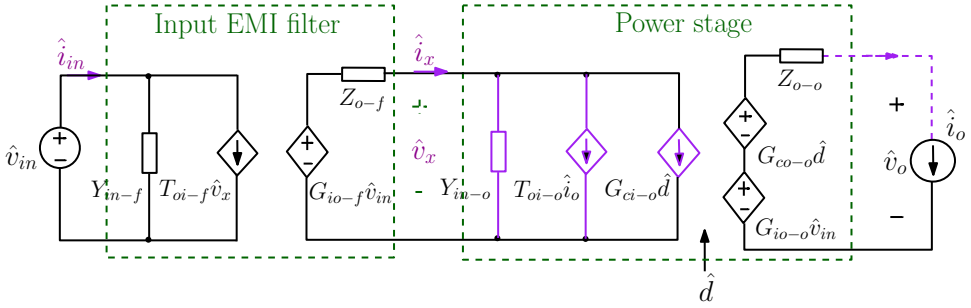


Figure 5.3. *Two-port model of the boost converter with an input EMI filter*

Based on the dynamic models expressed with the middle variable $(\hat{v}_x, \hat{i}_x)$ and the two-port model, the open loop input-filter-affected dynamic representations can be solved as [26, p. 237]:

$$\begin{bmatrix} \hat{i}_{in} \\ \hat{v}_o \end{bmatrix} = \begin{bmatrix} Y_{in-f} + \dfrac{G_{io-f}T_{oi-f}Y_{in-o}}{1+Z_{o-f}Y_{in-o}} & \dfrac{T_{oi-f}T_{oi-o}}{1+Z_{o-f}Y_{in-o}} & \dfrac{T_{oi-f}G_{ci-o}}{1+Z_{o-f}Y_{in-o}} \\ \dfrac{G_{io-f}G_{io-o}}{1+Z_{o-f}Y_{in-o}} & -\dfrac{1+Z_{o-f}Y_{in-sco}}{1+Z_{o-f}Y_{in-o}}Z_{o-o} & \dfrac{1+Z_{o-f}Y_{in-\infty}}{1+Z_{o-f}Y_{in-o}}G_{co-o} \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \\ \hat{i}_o \\ \hat{i}_{co} \end{bmatrix} \tag{5.8}$$

where Y_{in-sco} and $Y_{in-\infty}$ are the short-circuit and ideal input impedances of the boost converter, respectively.

5.2 Minor Loop Gain

When an input EMI filter is cascade-connected with a switched-mode converter, the impedance-based stability assessment method developed by Middlebrook for evaluating the stability of the cascaded system is applicable [11].

In the filter-converter interconnected system that studied in this thesis, the impedance ratio is defined as [26, p. 237]:

$$K_{minor} = Z_{o-f}Y_{in-c}^{ACM} = \frac{Z_{o-f}}{Z_{in-c}^{ACM}}$$

As stated in [18], the impedance ratio of the filter-affected converter is supposed to meet the Nyquist Stability Criterion (NSC) for stable operation of the interconnected system, which means the crucial point $(-1, 0)$ on the complex-plane can not be encircled in the Nyquist diagram of the impedance ratio when the subsystem does not include RHP-pole. Typically, this also indicates that the phase difference between two impedances is smaller than 180° at the crossover frequency of the impedance ratio ($f_{co-minor}$).

However, [14] found that it is inaccurate to determine the stability by finding the difference between the impedance-phase and 180° at frequency $f_{co-minor}$ only, because the direction of the Nyquist trajectory is neglected. Therefore, to ensure the stability by NSC, it is necessary to consider both the derivatives of magnitude and phase response at frequency $f_{co-minor}$ on bode plots [14].

6 SIMULATION RESULTS AND STABILITY ANALYSIS OF FILTER-CONVERTER INTERCONNECTED SYSTEM

The model of the filter-converter interconnected system with different filters for simulation is built in this chapter, where the ACM controlled boost converter that operates in CCM is utilized as the example case. The simulation results demonstrated the existence of filter-converter interactions as well as the effectiveness of predicting system stability with minor loop gain.

6.1 Simulation of Filter-Converter Interconnected System

The impedance-based stability assessment is typically applied to analyze the stability of the interconnected systems, more specifically, the NSC is utilized to the minor loop gain to decide the internal stability.

6.1.1 Simulink Model and Component Sizing of Input Filter

In this thesis, a single-section LC-type circuit is simulated and the corresponding Simulink model is given in Appendix A. It is used as the input EMI filter for the ACM-controlled boost converter. The Simulink model of the ACM-controlled boost converter connected with an input EMI filter is displayed in Appendix A, where the LC-type input filter is packed as a subsystem.

An improperly designed input filter will produce unnecessary volume, cost and compromise the performance of the whole system. The aim of the input EMI filter design is to keep a balance between the total performance and the size at a lower cost [24]. The input EMI filter performance depends mostly on the selection of the capacitor and inductor. In boost rectifiers, relative large capacitance and relative small inductance are required in the input EMI filter [25].

For the LC-type input EMI filter, its input-to-output transfer function is delivered as:

$$G_{iof}(s) = \frac{V_o(s)}{V_{in}(s)} = \frac{1 + sr_C C}{s^2 LC + s(r_L + r_C)C + 1} = \frac{\dfrac{1 + sr_C C}{LC}}{s^2 + s\dfrac{(r_L + r_C)}{L} + \dfrac{1}{LC}} \tag{6.1}$$

The damping factor ζ as well as characteristic undamped natural frequency ω_n of the input EMI filter is found by comparing the denominator of $G_{iof}(s)$ with the denominator of generalized second-order transfer function in Equation 2.25:

$$\begin{aligned} &\text{Undamped natural frequency: } \omega_n = \frac{1}{\sqrt{L_f C_f}} \\ &\text{Damping factor: } \zeta = \frac{r_{Lf} + r_{Cf}}{2}\sqrt{\frac{C_f}{L_f}} \\ &\text{Resonant frequency: } \omega_{res} = \omega_n\sqrt{1 - 2\zeta^2} \end{aligned} \tag{6.2}$$

The damping ratio (ζ) of the input filter is normally quite small because the resistances are low and the value of $\dfrac{C_f}{L_f}$ is usually less than 1, this small damping ratio causes harmonics that near f_s in the output current of the input EMI filter, which results in oscillations near the resonant

frequency, and eventually make the converter unstable. Therefore, the damping ratio of the input EMI filter should be increased to prevent the input current oscillation. [25]

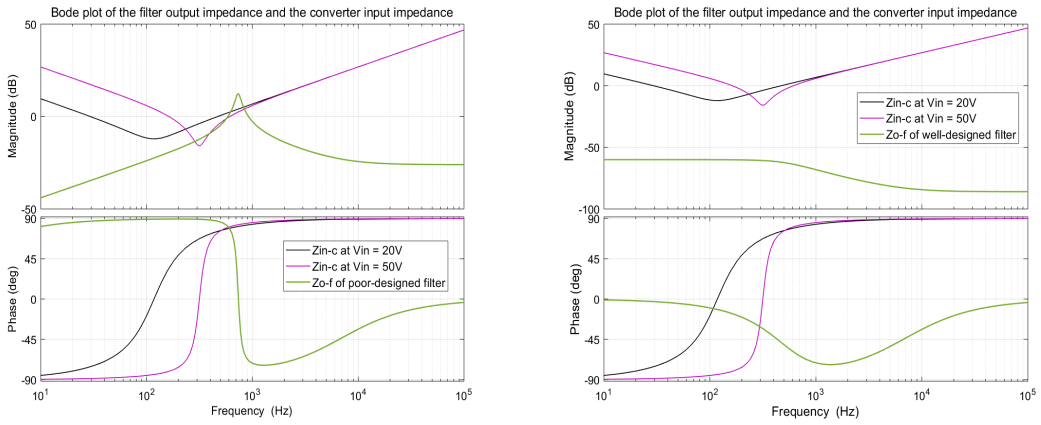
According to the extra element theorem provided in [20], the control loop gain of the switched-mode converter is unlikely to be modified considerably by the input EMI filter as long as the input impedance curve of the converter is far above the peak output impedance curve of the filter. Therefore, the filter peak output impedance should be placed carefully to avoid resulting oscillations in the transient performance. From a design perspective, a damping ratio more than $\frac{1}{\sqrt{2}}$ (i.e., 0.7) is feasible for obtaining a proper filter size as well as a favorable control performance [24].

In order to show the effects of filter-converter interactions, a poor-designed and a well-designed filter are constructed and their impacts on the interconnected system are compared. The values of the input EMI filter components are epitomized in Table 6.1.

Table 6.1. *Component Parameters used for Input Filter Simulation.*

Input filter parameters			
Poor-designed input filter		Well-designed input filter	
Filter Inductor (L_f)	$100\mu H$	Filter Inductor (L_f)	$0.2\mu H$
ESR of inductor (r_{Lf})	$1m\Omega$	ESR of inductor (r_{Lf})	$1m\Omega$
Filter Capacitor (C_f)	$470\mu F$	Filter Capacitor (C_f)	$470mF$
ESR of capacitor (r_{Cf})	$50m\Omega$	ESR of capacitor (r_{Cf})	$50\mu\Omega$
Damping ratio (ζ)	0.0553	Damping ratio (ζ)	0.8048

6.1.2 Simulation Results with Different Input Filters



(a) *Poor-designed filter* ***(b)*** *Well-designed filter*

Figure 6.1. *Bode plot of the boost converter input impedance and output impedance of different filters at varying* V_{in}

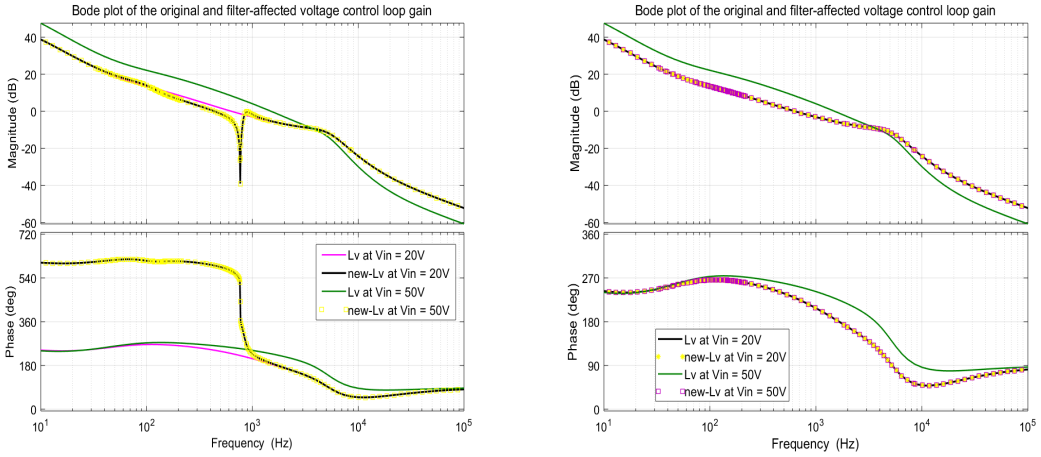
With the parameters defined in Table 6.1, the bode diagrams of different filter output impedance at varying input voltages are illustrated in Figure 6.1. As [20] presented, the control loop gain would not be affected considerably by the input filter as long as the curve of converter input impedance is far above the input EMI filter output impedance curve, the well-designed input filter displayed in Figure 6.1b conform with this principle.

The voltage control loop gain of ACM-controlled boost converter is modified by the input filter

design, yields filter-affected control loop gain:

$$L_{v-f} = \frac{1 + Z_{o-f} Y_{in-\infty-o}}{1 + Z_{o-f} Y_{in-o}} L_v \tag{6.3}$$

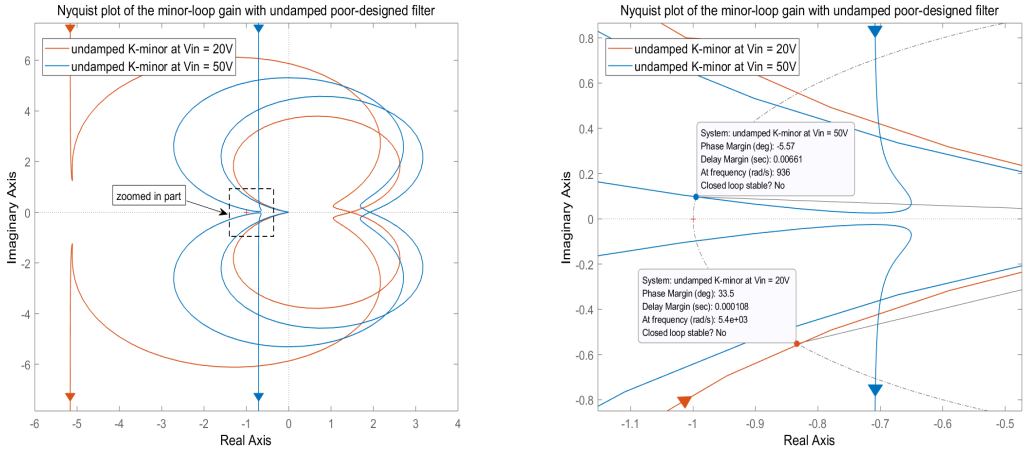
where $Y_{in-\infty} = Y_{in-o} - \dfrac{G_{io-o} G_{ci-o}}{G_{co-o}}$.



(a) *With poor-designed filter* ***(b)*** *With well-designed filter*

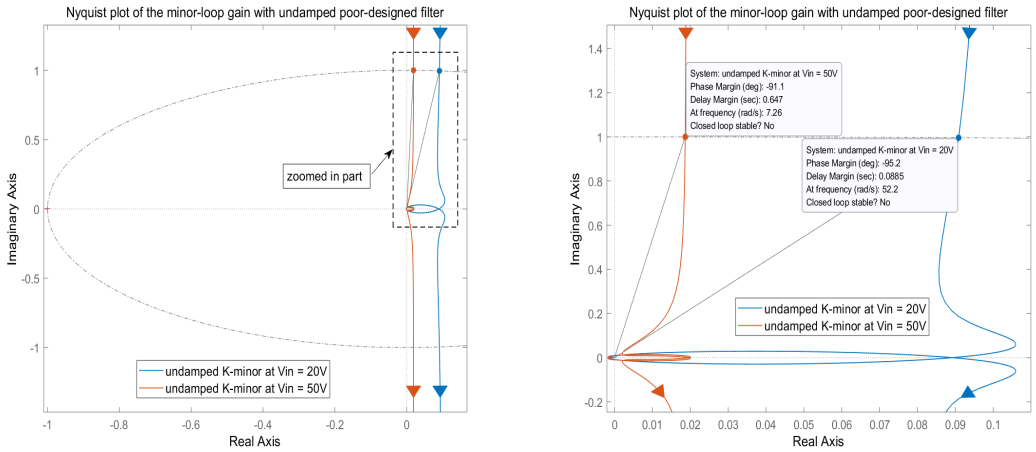
Figure 6.2. *Bode plot of the original and filter-affected control loop gain at varying input voltage*

Figure 6.2a and 6.2b illustrated the bode plots of the original and filter-affected control loop gain with poor-designed and well-designed input filter, respectively. A comparison of these two figures shows that a poor-designed input filter affects the control loop gain significantly while the well-designed input filter does not, and this effect is enhanced slightly as the input voltage increases. Figure 6.2a also implies that the output voltage transient performance would oscillate due to the big dip at a frequency around $780Hz$ in the poor-designed filter-affected control loop gain. In contrast, the corresponding transient response may be unchanged because the well-designed filter does not cause significant change to the control loop gain.



(a) *Zoomed out Nyquist plot* ***(b)*** *Zoomed in Nyquist plot*

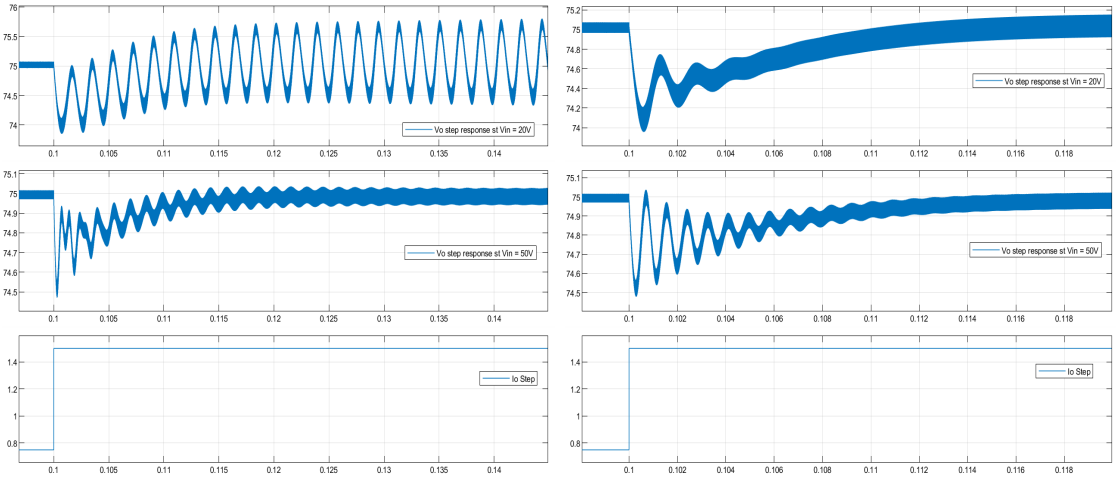
Figure 6.3. *Nyquist plot of the poor-designed filter-affected minor loop gain at varying* V_{in}



(a) *Zoomed out Nyquist plot* ***(b)*** *Zoomed in Nyquist plot*

Figure 6.4. *Nyquist plot of the well-designed filter-affected minor loop gain at varying* V_{in}

With the minor-loop gain (K_{minor}), the stability of the interconnected system can be easily evaluated. Nyquist plots of K_{minor} of the converter with different filters are depicted in Figure 6.3 where the filter is poor-designed, and in Figure 6.4 where the filter is well-designed. It is clear to see that the Nyquist curve of both the impedance ratio is not encircling (-1,0) point, which guarantees the stability of the cascaded system. However, the PM of the interconnected system with poor-designed input filter at $V_{in} = 20V$ is $33.5°$ in Figure 6.3, which is lower than the stable margin $40°$. This implies that the transient performance of the boost converter will be degraded. In addition, the PM of the minor loop gain displayed in Figure 6.4 is adequate for the system to obtain a desirable control performance.



(a) *With poor-designed input filter* ***(b)*** *With well-designed input filter*

Figure 6.5. *Output voltage step response of the boost converter with different input filters*

The transient response of the switched-mode boost converter influenced by the poor-designed input EMI filter is illustrated in Figure 6.5, the step response at different input voltage are both stabilized at $75V$ but contains resonance, which matches the prediction of the minor loop gain Nyquist plots. The performance degradation at different input voltages is due to the large dip in the filter-affected control loop gain. In other words, the poor-designed input filter destroys the control performance of the converter. On the contrary, the step response of the interconnected system is generally unaffected if the filter is well-designed as shown in Figure 6.5b, which has been also indicated by the Nyquist diagram of the minor loop gain. Moreover, the setting time of the step response with a well-designed filter (approximately $0.014s$) is lower than it with poor-

designed filter (approximately $0.03s$), which implies that an improperly designed filter slows down the control performance.

6.2 Damping Circuit

As shown in Section 6.1.2, a poorly designed input filter may destroy the frequency response performance and even cause stability issues [34]. Without proper damping, an input filter will lead to a peak near its resonant frequency in the transient response, which means the noise signal is actually amplified instead of reduced [34]. This section presents the system response with a damping circuit.

6.2.1 Damping Circuit Design

One way to enhance the control performance is to damp the filter resonance by adding a damping RC circuit at the input terminal of the converter. The high power consumption produced by the damping resistor (R_d) can be solved by connecting an extra bipolar capacitor (C_d) in series with R_d [25]. Figure 6.6 shows the corresponding circuit schematics.

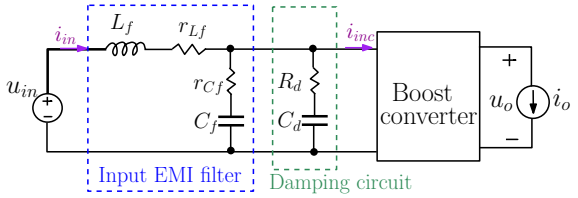


Figure 6.6. *Circuit schematics of DC-DC boost converter with input filter and damping circuit*

According to the circuit schematics, the model of the ACM-controlled boost converter with damped-filter built in Simulink is illustrated in Appendix A, where the input EMI filter and damping circuit are packed as a subsystem as given in Appendix A.

The transfer function Z_3 in the Simulink model of damped input filter is calculated as:

$$\begin{aligned}
&\text{Input filter inductance: } Z_1 = r_{L-f} + sL_f \\
&\text{Input filter capacitance: } Z_2 = r_{C-f} + \frac{1}{sC_f} \\
&\text{Damping circuit impedance: } Z_{damp} = R_d + \frac{1}{sC_d} \\
&\text{Filter capacitance in parallel with damping impedance: } Z_3 = \frac{Z_2 Z_{damp}}{Z_2 + Z_{damp}}
\end{aligned} \tag{6.4}$$

The function of the damping capacitor (C_d) is to solve the power dissipation problem on the resistor, and the damping resistor is used to decrease the peak of the filter output impedance at the resonant frequency. The capacitor value (C_d) should be larger than the filter capacitor (C_f) for avoiding affecting the cutoff point of the input filter while R_d should be lower than the filter output impedance at f_{res} [24]. Based on these limitations, the damping circuit parameters can be calculated as below.

$$\begin{aligned}
R_d &= \sqrt{\frac{L_f}{C_f}} \\
C_d &= 4C_f
\end{aligned} \tag{6.5}$$

The used values of the damping circuit components are summarized in Table 6.2.

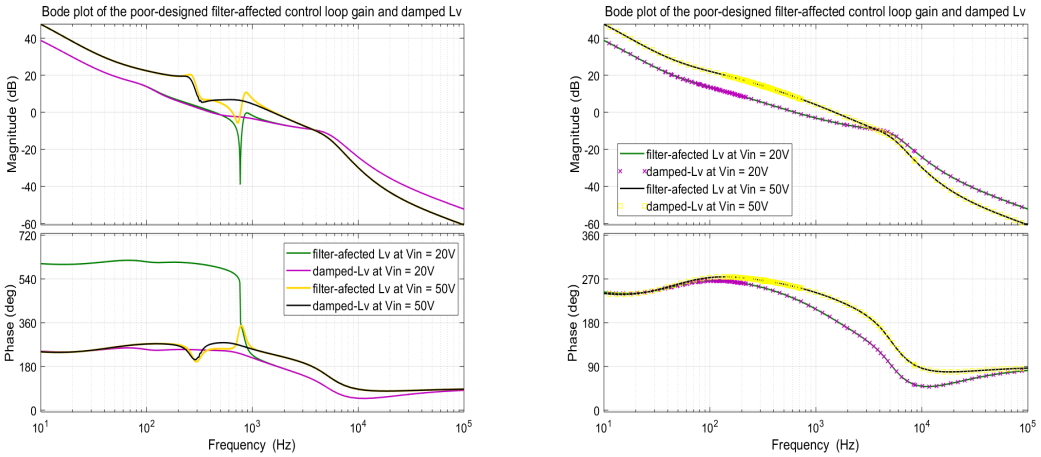
Table 6.2. *Component Parameters used for Damping Circuit Simulation.*

Damping parameters for poor-designed filter		Damping parameters for well-designed filter	
Damping Capacitor (C_d)	$1.9mF$	Damping Capacitor (C_d)	$1.88F$
Damping Resistor (R_d)	$461.3m\Omega$	Damping Resistor (R_d)	$65.233m\Omega$

6.2.2 Simulation Results with a Damping Circuit

By using the total output impedance including the damping circuit and input filter, the damped-filter-affected voltage feedback control loop gain can be computed as:

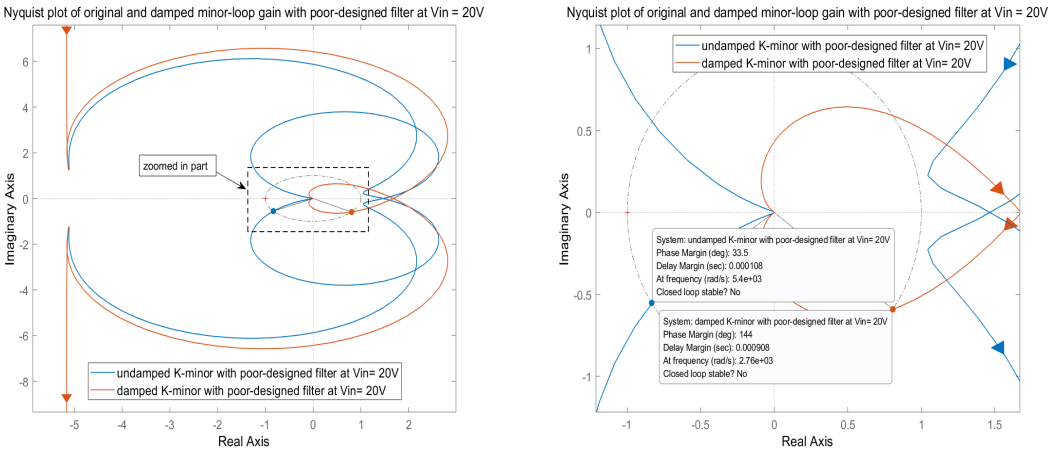
$$\begin{aligned} &\text{Total impedance of the damped-input-filter: } Z_{of-damp} = \frac{Z_1 Z_3}{Z_1 + Z_3} \\ &\text{Damped-filter-affected control loop gain: } L_{v-damped} = \frac{1 + Z_{of-damp} Y_{in-\infty-o}}{1 + Z_{of-damp} Y_{in-o}} L_v \end{aligned} \tag{6.6}$$



(a) *With poor-designed filter* ***(b)*** *With well-designed filter*

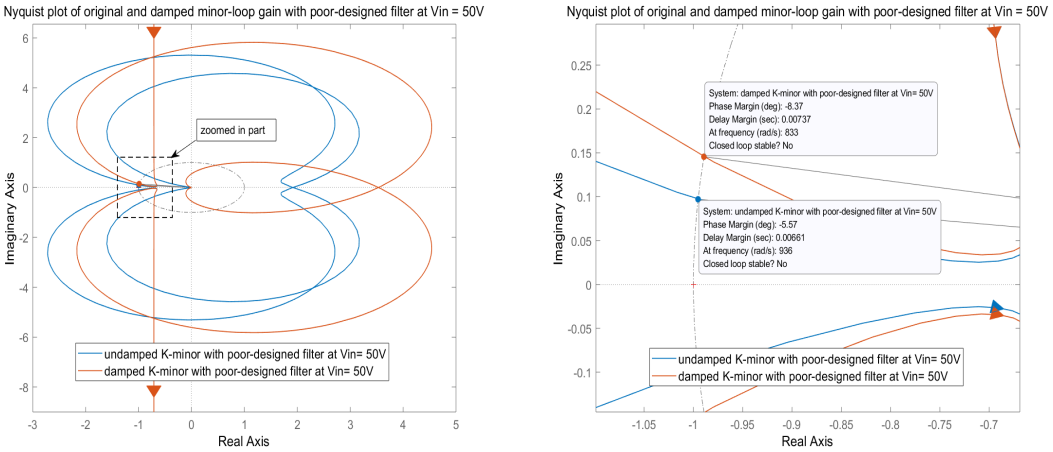
Figure 6.7. *Bode plot of the undamped and damped-filter-affected control loop gain with different filters*

The corresponding bode plots of the undamped and damped filter-affected control loop gain at varying input voltage with different filter sizes are displayed in Figure 6.7. It is evident that the dip in the loop gain caused by the poor-designed filter are both effectively removed at varying input voltage. By comparison, the damped-filter-affected control loop gain with a well-designed filter is basically unaffected, because there is no big resonance to be damped in the original undamped-filter-affected control loop gain.



***(a)** Zoomed out Nyquist plot* ***(b)** Zoomed in Nyquist plot*

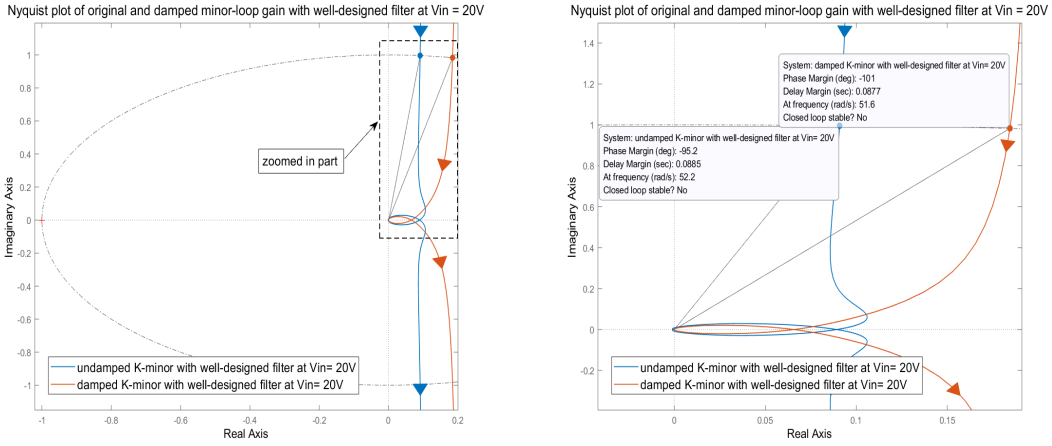
***Figure 6.8.** Nyquist plot of the undamped and damped minor loop gain with poor-designed filter at input voltage of $20V$*



***(a)** Zoomed out Nyquist plot* ***(b)** Zoomed in Nyquist plot*

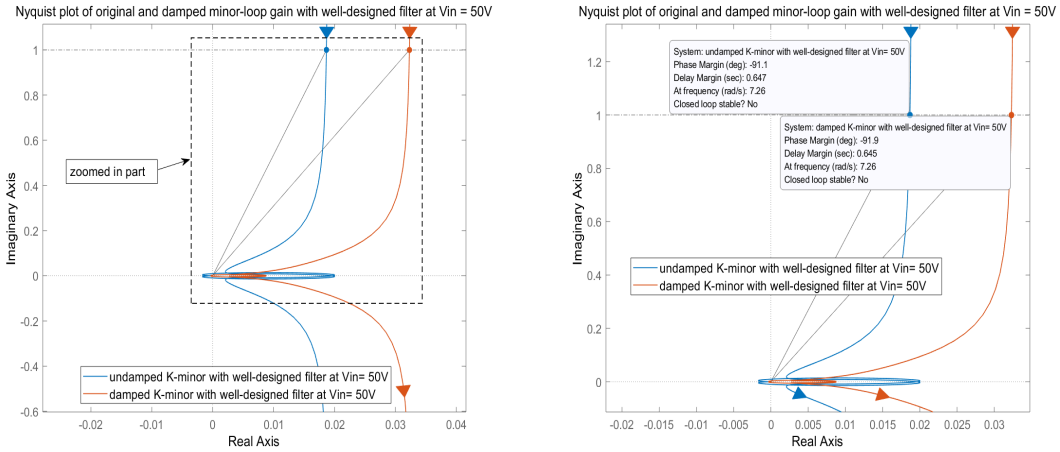
***Figure 6.9.** Nyquist plot of the undamped and damped minor loop gain with poor-designed filter at input voltage of $50V$*

Figure 6.8 and 6.9 illustrated the Nyquist plot of the undamped and damped impedance ratio with poor-designed filter at $V_{in} = 20V$ as well as $V_{in} = 50V$, respectively. The original minor loop gain of the cascade-connected system with a poor-designed filter is lower than $40°$ at an input voltage of $20V$, which implies the oscillations in the step response. Nevertheless, the PM is improved significantly (from $33.5°$ to $144°$) with the damping circuit, therefore the resonance in the transient performance is ought to be damped.



***(a)** Zoomed out Nyquist plot* ***(b)** Zoomed in Nyquist plot*

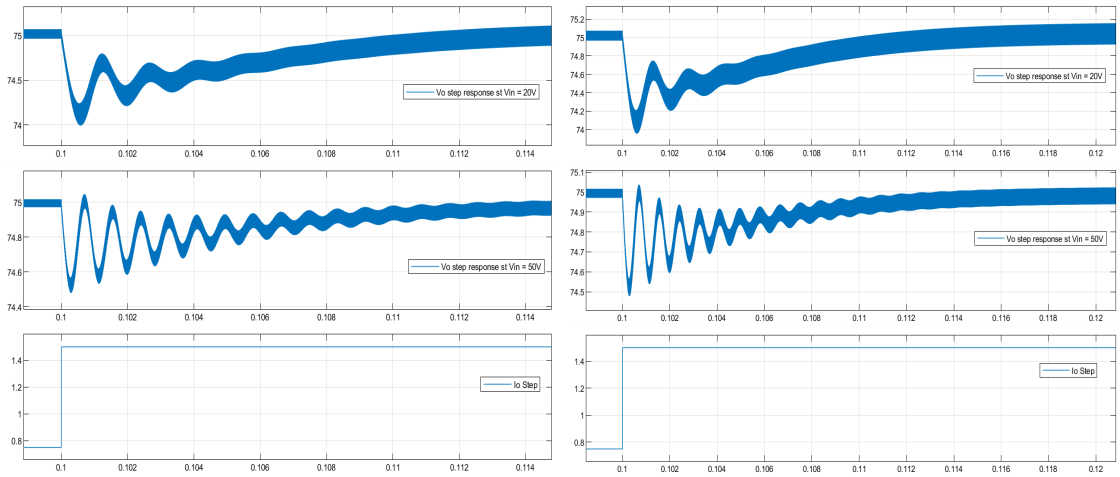
***Figure 6.10.** Nyquist plot of the undamped and damped minor loop gain with the well-designed filter at input voltage of* $20V$



***(a)** Zoomed out Nyquist plot* ***(b)** Zoomed in Nyquist plot*

***Figure 6.11.** Nyquist plot of the undamped and damped minor loop gain with the well-designed filter at input voltage of* $50V$

On the other hand, the Nyquist diagrams of the undamped and damped minor loop gain with the well-designed filter at $V_{in} = 20V$ as well as $V_{in} = 50V$ are displayed in Figure 6.10 and 6.11, respectively. The PM of the damped minor loop gain are both increased slightly. In other words, the interconnected system is already stable with an undamped-well-designed filter, the damping circuit might somewhat improve the performance but does not make a big difference to the system.



(a) *With damped poor-designed input filter* ***(b)*** *With damped well-designed input filter*

Figure 6.12. *Output voltage step response of the DC-DC boost converter with damped input filter*

Figure 6.12a illustrates the output voltage transient performance with a damped poor-designed filter, where the oscillation is significantly damped compared to the step response with undamped one. By contrast, in the case of the well-designed filter, as shown in Figure 6.12b, the transient performance with and without damping circuit is generally the same, because the control loop gain is roughly unaffected.

This chapter clearly illustrated the effect of filter design on the control performance as well as the damping capability of the RC damping circuit. Furthermore, the above simulation results demonstrated the effectiveness of applying the impedance ratio to identify the stability of the interconnected system, founded on the fact that the transient response is basically conformed with the predictions of the Nyquist plots.

7 CONCLUSION

This thesis presented the impact of the design of the input filter on a filter-converter interconnected system in depth and a case study is utilized to examine the theoretical analysis. The main target of this thesis is achieved by deriving the detailed dynamic models as well as analyzing the stability of a filter-affected converter based on an ACM controlled DC-DC boost converter that operates in CCM. Small-signal models for representing the dynamic behaviors of the voltage-fed boost converter under both DDR and ACM control are provided in detail with the help of the control block diagram and control loop gain identification. The obtained small-signal models are a useful tool for control design as well as stability analysis.

On the basis of the dynamic models, Chapter 4 reported thoroughly the design process of DDR and ACM control for boost converter in the Simulink environment. The compensated control loop gain achieved the desired performance for stabilizing the converter operation. The obtained frequency response provided relative accurate predictions for the transient response, which further verified the correctness of the small-signal models. For instance, the output voltage dip difference in transient performance at varying input voltage is hinted in the frequency response of the output impedance. However, the slight difference ($0.6129V$ at $V_{in} = 20V$ and $0.3085V$ at $V_{in} = 50V$ under ACM control) between the predicted voltage dip and the simulated dip value shows that the accuracy of the small-signal model is inadequate.

Although the feedback controller is tuned properly, the system stability is also influenced by external disturbances such as the input EMI filter. Hence, the impedance ratio for evaluating the stability of this filter-converter interconnected system is computed in Chapter 5. For the purpose of displaying the impact of filter designing to the control performance, a poor-designed filter and a well-designed filter are designed and the corresponding system stability is well forecasted by the minor loop gain. The simulation results demonstrated that the poor-designed filter does have a significant effect on the system because it modifies the shape of the control loop gain considerably (i.e., the big dip in the Bode plot of the filter-affected control loop gain). Although the interconnected system is still stable as long as the complex point (-1,0) was not encircled in the Nyquist plots of the impedance ratio, the low PM (33.5° at $V_{in} = 20V$) of the poor-designed filter implies performance degradation, which is validated by the undesirable transient response. In contrast, the shape of the control loop gain would not be changed to a large extent when the filter is well-designed, thus the transient performance is well regulated by the controller. Furthermore, damping circuits for different filters are designed for dealing with filter-converter interactions. The results from simulation in Chapter 6 illustrated that the oscillations in the transient response are perfectly damped, especially the big oscillations caused by the poor-designed filter, since the PM of Nyquist plot of damped-filter-affected impedance ratio is significantly improved from 33.5° to 144° at $V_{in} = 20V$, and the big dips in the Bode plot of the damped-filter-affected control loop gain is effectively removed.

In summary, the simulation results are in compliance with theoretical predictions in general. This thesis mainly studied in the CCM of the switched-mode DC-DC boost converter with DDR and ACM control. However, there are other basic and higher-order converter topologies that are not mentioned in this paper. Therefore, dynamic models of other converter layouts operating in DCM, and controlled with different control schemes should be investigated in the future. In addition, different input filters and damping circuit topologies could be applied as well, which is also left to future work.

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A SIMULINK MODELS

The Simulink models used in this thesis are displayed in this Appendix.

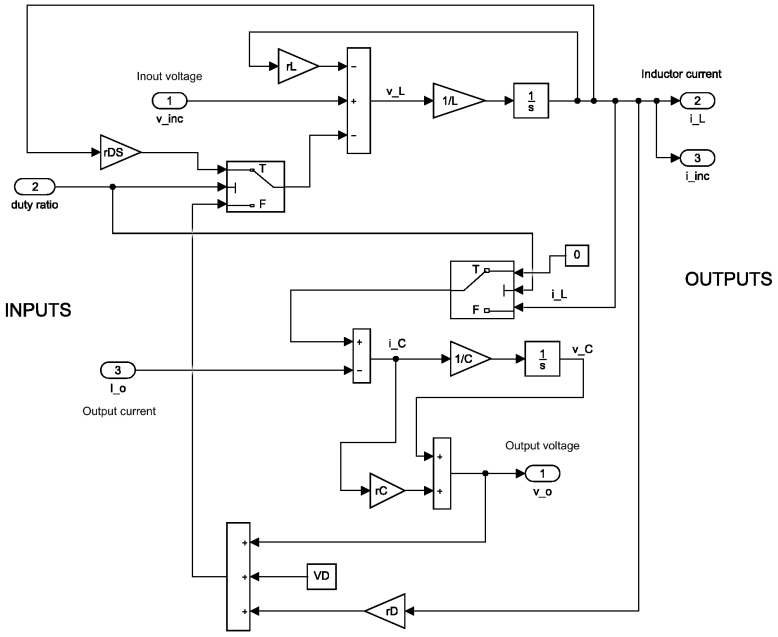

Figure A.1. *Simulink model of the power stage of boost converter*

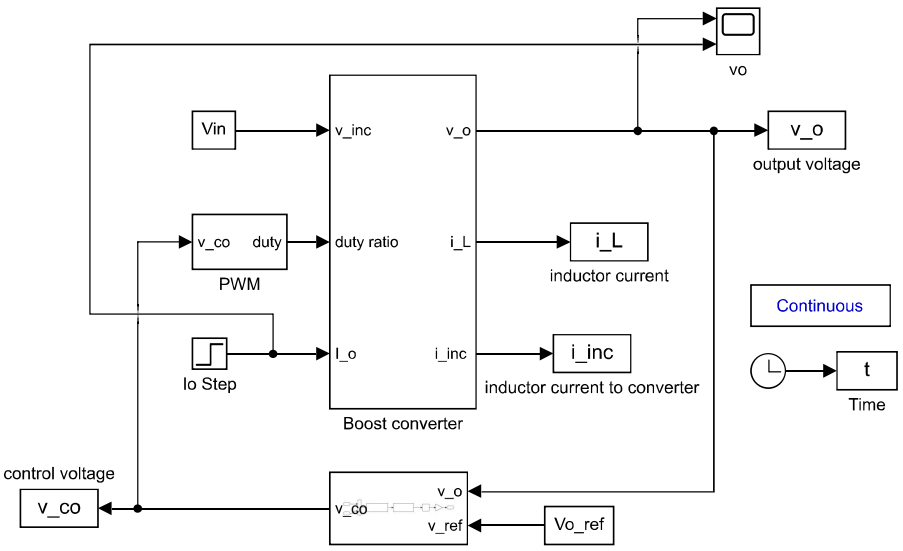

Figure A.2. *Simulink model of the DDR controlled boost converter*

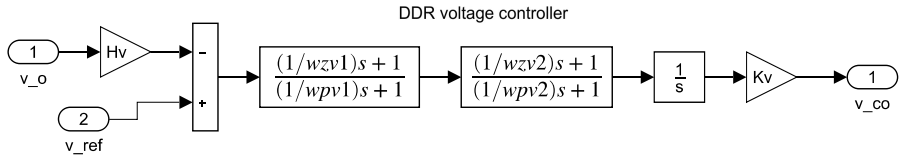

Figure A.3. *Simulink model of the voltage compensator of DDR controlled boost converter*

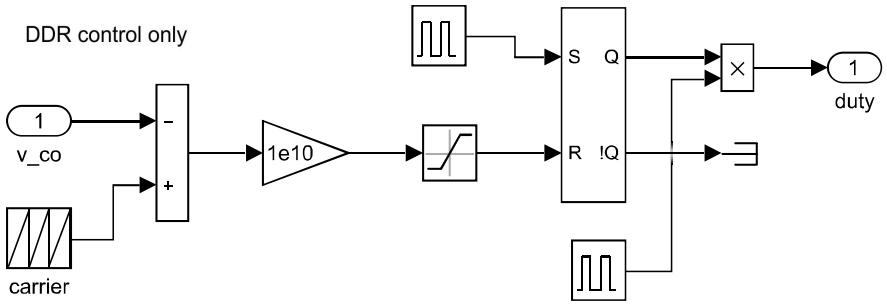

Figure A.4. *Simulink model of the PWM modulator of DDR controlled boost converter*

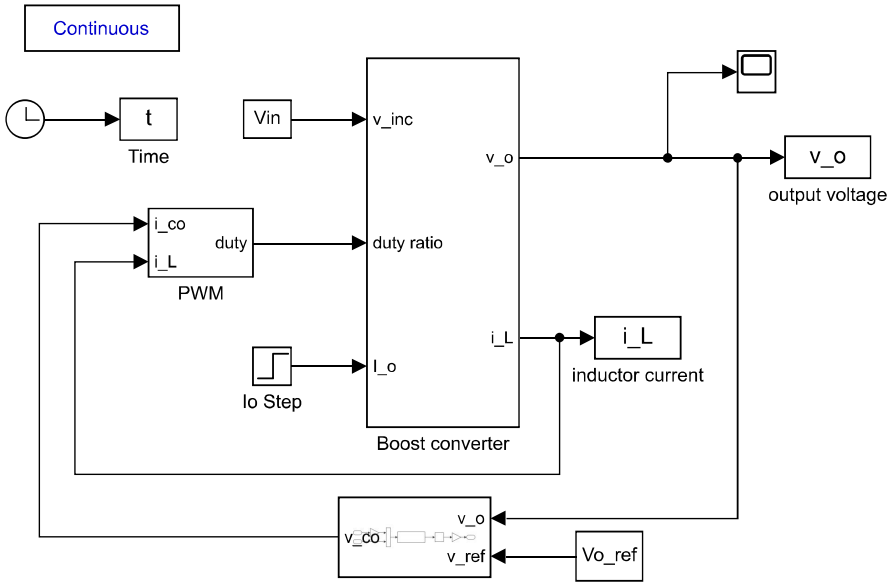

Figure A.5. *Simulink model of the boost converter under Average-current-mode control*

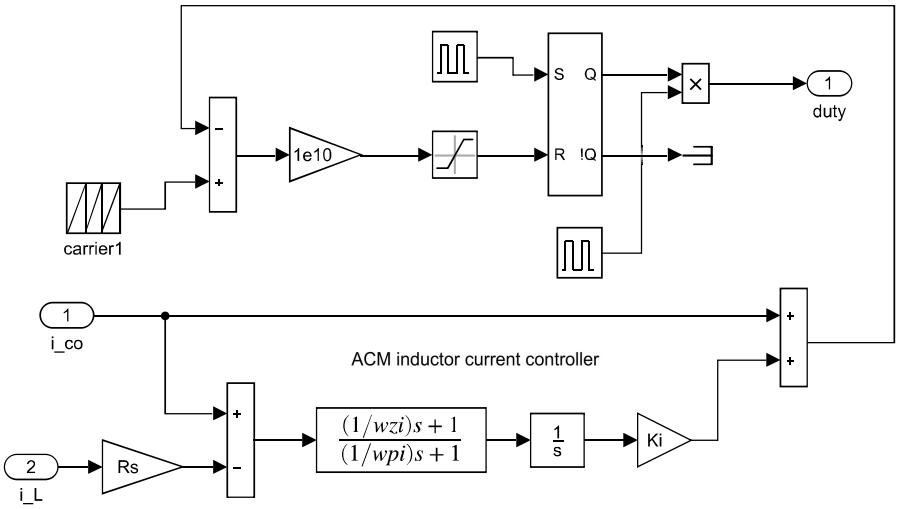

Figure A.6. *Simulink model of the inner current compensator and PWM modulator of ACM controlled boost converter*

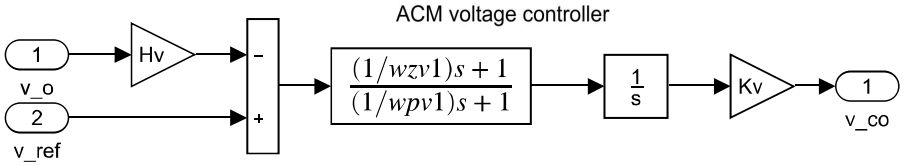

Figure A.7. *Simulink model of the outer voltage compensator of ACM controlled boost converter*

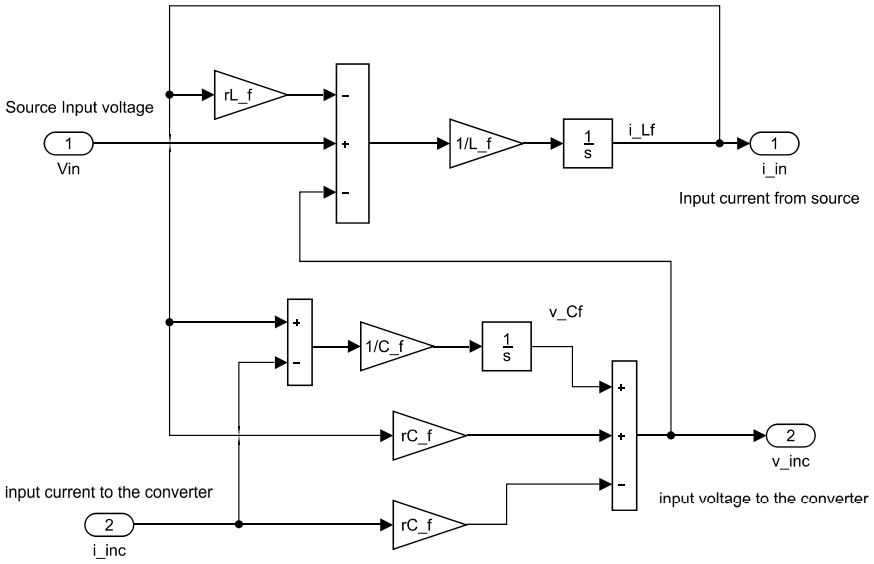

Figure A.8. *Simulink model of the input EMI filter*

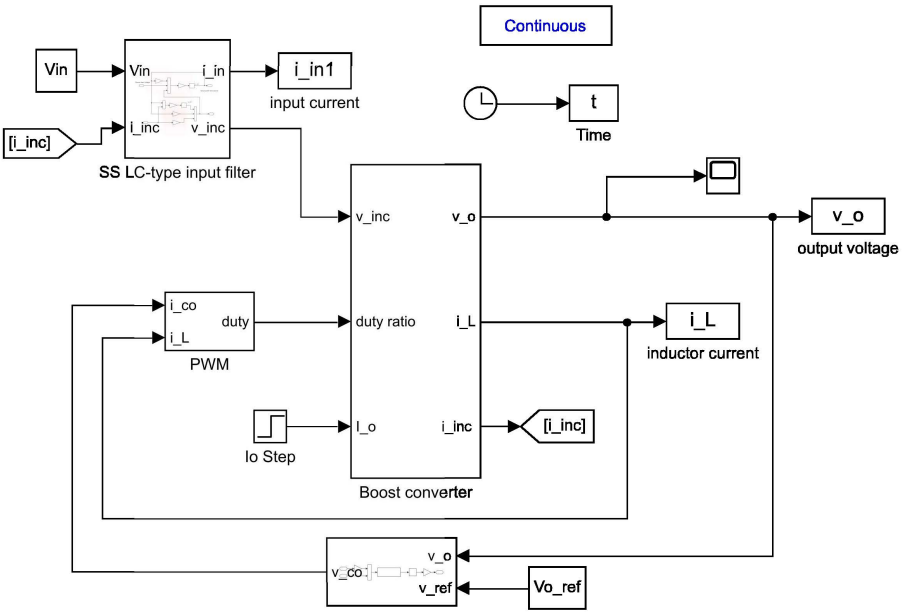

Figure A.9. *Simulink model of the ACM controlled boost converter connected with an input filter*

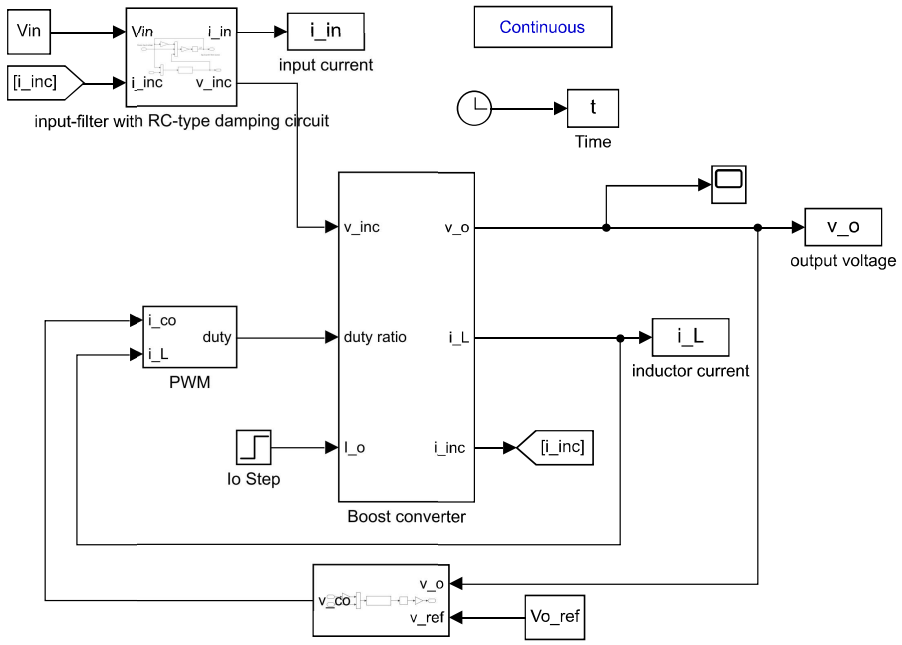

Figure A.10. *Simulink model of ACM controlled boost converter with damped-input-filter*

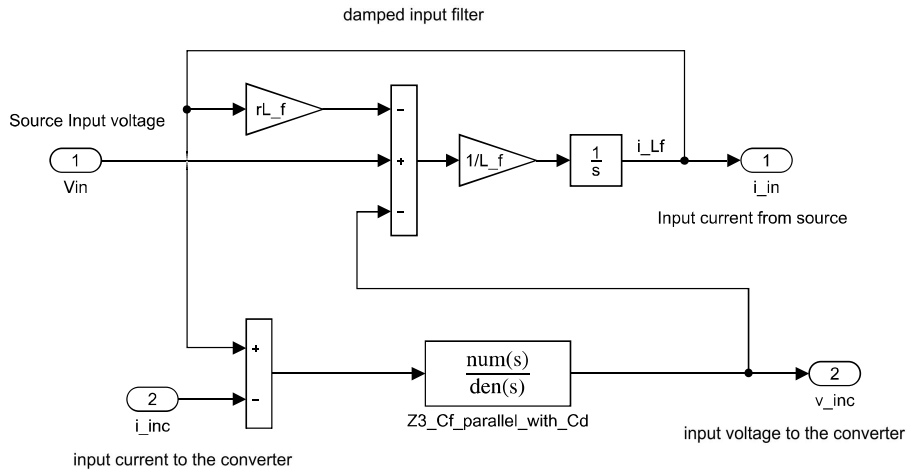

Figure A.11. *Simulink model of the input filter and damping circuit as a subsystem*